Generalized Implementation of Switching-Loss-Minimized Space-Vector Modulation for Three-Level Converters

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***Abstract*—With increasing integration of the intermittent and volatile renewable energy resources into the existing ac grid infrastructure, the grid stability is decreasing. Large battery storage systems are proposed to act as short-time buffer to cope with transient instabilities. A promising converter to interface such low-voltage high-power battery banks is the T-type Neutral-Point-Clamped Converter (TNPC). A generalized implementation of a variant of the well-known space vector modulation featuring lower losses is proposed in this work. The derived relations to select a particular switching sequence are based on the binary logic and symmetry of the possible states in such a three-level converter. The algorithm proposed in this work dynamically adjusts the switching sequences to accommodate capacitive as well as inductive behavior.**

***Index Terms*—Neutral-point-clamped (NPC) converters, T-type NPC (TNPC), pulse-width modulation (PWM), space-vector modulation (SVM), bus clamping**

I. Introduction

Pulse-width modulation (PWM) is one of the most widely researched and implemented technique over the past three decades [1] to control the output parameters of a converter. In this technique, which is adapted from the well-established communication theory [2], the pulse-width or the on-time of power switches is controlled at high speed to generate a low-frequency output quantity [3]. The choice of the modulation strategy is one of the most crucial steps in a converter design. The modulation strategy can have a great impact on the converter efficiency [4], [5].

Different PWM schemes can be evaluated based on the resulting harmonic content, dc bus utilization, losses and the switch utilization. Since the inception of carrier-based PWM, a huge volume of literature has been written about the improvements and variants to address these aspects. This includes but is not limited to interleaving the carriers for better harmonic performance and paralleling inverters [6], [7] and using random carrier signals [8] instead of deterministic ones as in conventional PWM. In order to implement the PWM in digital hardware, the space vector modulation (SVM) was developed by [9] which was later extended to the three-level neutral-point-clamped (NPC) converter [10], [11]. The SVM not only increases the dc bus utilization as compared to classical carrier-based PWM but also enables to influence other aspects of a three-level converter such as common-mode voltage and neutral-point current [12]. SVM also provides a possibility to reduce the effective switching frequency by not switching certain devices for certain period of time to reduce switching losses [13], [14].

In this paper, the ability of SVM to clamp certain devices for a fraction of the fundamental cycle to reduce switching losses is used. The clamping window is dynamically adjusted in order to obtain the maximum benefit of reduced switching losses around the current peak. Unlike conventional implementations through look-up tables or state machines, a generalized algorithm has been developed through matrix manipulation and basic binary logic operations to determine the optimal switching sequence and state. The chosen converter topology is that of the T-type NPC converter [15], [16].

After this introduction, a brief overview of the existing modulation schemes is given for the sake of completion. Thereafter, the developed algorithm is presented in detail followed by the simulation results and conclusions.

II. Pulse-Width Modulation (PWM) Techniques

In this work, the three-level T-type neutral-point-clamped (TNPC) converter is considered for connecting a large battery bank to the grid. An LCL filter is used at the output of the converter to comply with the grid codes, as shown in Figure 1. A brief description of the modulation schemes for such a converter is given in following sections.

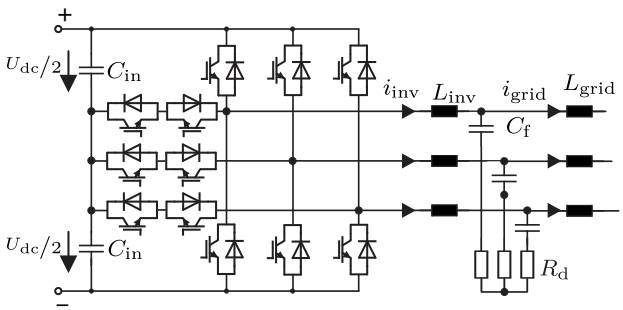


Figure 1: T-type neutral-point clamped converter

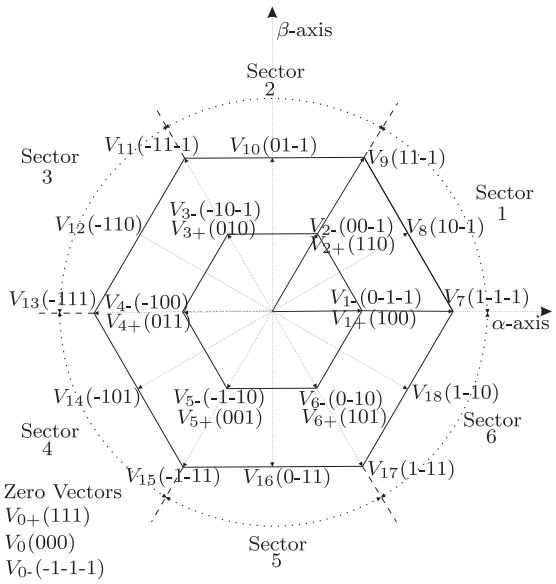


Figure 2: Sectors of SVM

A. Sine-triangle Pulse-Width Modulation (SPWM)

The PWM technique works by varying the duty cycle (d) of the switches of the converter at a high frequency compared to the fundamental frequency. The duty cycle and the exact switching instants are determined by comparing a low-frequency reference waveform u_{ref} with a high-frequency carrier waveform u_{car}. The switching rule can be written as follows:

$$u_{\mathrm{car}} > u_{\mathrm{ref}} \Rightarrow S = 1 \qquad \text{otherwise} \qquad S = 0 \qquad (1)$$

where $S = 1$ means that the corresponding device is gated on and vice versa. The reference waveform in inverter applications is often sinusoidal. The carrier waveform could be sawtooth or triangular. As the harmonic performance of the latter is better [1], it is commonly used in the industry and hence, the name Sine-triangle PWM (SPWM).

For a given dc-link voltage U_{dc} and a reference voltage u_{ref} the amplitude of the fundamental component of the output voltage ${}^1\widehat{U}_{\mathrm{o}}$ of any phase leg with respect to the mid-point of the dc-link is given as [1]:

$${}^1\hat{U}_{\mathrm{o}} = \frac{\hat{u}_{\mathrm{ref}}}{\hat{u}_{\mathrm{car}}} \cdot \frac{U_{\mathrm{dc}}}{2} = m \cdot \frac{U_{\mathrm{dc}}}{2} \qquad (2)$$

with $m = \widehat{u}_{\mathrm{ref}}/\widehat{u}_{\mathrm{car}}$ being the modulation index. The ${}^1\widehat{U}_{\mathrm{o}}$ varies linearly with modulation index up to $m = 1$. Beyond this region, the inverter is said to be over-modulated. Over-modulation is generally avoided for simpler control and better harmonic performance.

B. Third-Harmonic-Injected Sine-triangle PWM (THI-SPWM)

When a third-harmonic component is added to the sinusoidal reference in PWM, it is possible to go beyond the modulation index of 1, without operating in the over-modulation region. As the third-harmonic components are identical for the three phases, they do not appear in the line-line voltages.

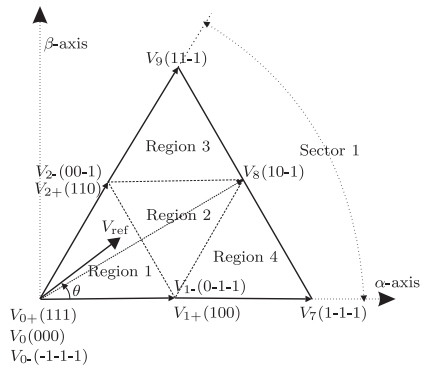


Figure 3: Sector 1 of SVM

The magnitude of the third-harmonic component injected is generally a fourth or a sixth of the fundamental reference wave, thus, achieving a modulation index of 1.12 and 1.15 respectively [1].

C. Space Vector Modulation (SVM)

In the SPWM and THI-SPWM techniques, the position of the pulses is determined by the algorithm and there is no degree of freedom to position the pulses and zero states in order to achieve better harmonic performance. Also, it is difficult to implement these techniques in digital hardware. To overcome these issues, space vector modulation (SVM) was introduced [9].

SVM is based on the fact that three-phase quantities can be transformed into a stationary two-dimensional $\alpha\beta$-system and represented as space vectors [9]. Each space vector corresponds to at least one inverter state. Each leg of a three-phase three-level inverter has three states, i.e. positive (1), zero (0) and negative (-1). A three-level three-phase inverter therefore, has a total of $3^3 = 27$ states [17]. The space vector diagram for a three-phase three-level inverter is given in Figure 2. The vectors that form the vertices of the inner hexagon, i.e. $V_{1+}...V_{6+}$ are short vectors each having two redundant states. The presence of this redundancy provides the flexibility of positioning various states to optimize certain aspect of the converter [12]. The outer hexagon can be divided into six identical sectors as shown in Figure 2. Each of the sectors can be further divided into four identical regions (triangles) as shown in the Figure 3. A reference vector V_{ref} can be generated by time-averaging two or more of these space vectors in one switching period.

D. Switching-Loss Minimized Space Vector Modulation (SLM-SVM)

As the switching frequency increases, the switching losses increase proportionally and the system efficiency decreases. Reference [18] proposed a variant of SVM that can reduce the switching losses by at least 33%. This technique makes use of the degree of freedom in choosing the zero and redundant states in SVM strategy. Accordingly, each phase is not switched for a certain interval of time in the switching period and is therefore, left connected to either the positive

TABLE I: Possible clamping intervals for different phases

Clamping interval	+ve clamped	-ve clamped
$0° \leq \theta \leq 60°$	Phase a	Phase c
$60° \leq \theta \leq 120°$	Phase b	Phase c
$120° \leq \theta \leq 180°$	Phase b	Phase a
$180° \leq \theta \leq 240°$	Phase c	Phase a
$240° \leq \theta \leq 300°$	Phase c	Phase b
$300° \leq \theta \leq 360°$	Phase a	Phase b

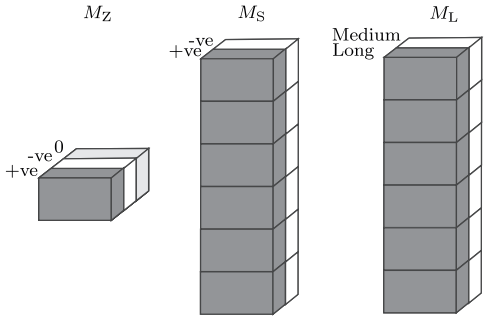


Figure 4: Matrices for SLM-SVM

or the negative rail. This reduces the effective number of commutations and hence, the switching loss.

The principle of SLM-SVM can be elaborated using Figure 2. Considering α-axis as the reference for all angle measurements, in the interval $300° \leq \theta \leq 60°$, the vertices on the outer hexagon are (1-11), (1-10), (1-1-1), (10-1), (11-1) which indicate that the phase a remains positive throughout this interval. Similarly, the vertices on the inner hexagon, (101)/(0-10), (100)/(0-1-1), (110)/(00-1) and the zero vectors (111)/(000)/(-1-1-1) each contain one state where phase a is positive. So, phase a can be connected to the positive bus in this interval. Similar observations can be made for other phases in other sectors as well. As the output waveforms of the different phases have a flat top during the respective intervals, this modulation technique is also called flat-top SVM [19]. These possible clamping intervals are summarized in Table I. It is to be noted that the maximum interval for which the phases can be clamped to either +ve or -ve dc-bus voltage is 120° and hence, the name 120° flat-top SVM. Since only one of the redundant states is used for 120°, the corresponding capacitor of the dc bus tends to discharge resulting in large fluctuations in the mid-point voltage necessitating the use of bigger dc-link capacitors. Moreover, the losses in the top and the bottom switches of the phase leg are not symmetrically distributed.

In order to manage the problems of 120° flat-top SVM, the clamping intervals can be split into two 60° subintervals. By clamping alternately to the positive and the negative rails for 60° subintervals, the dc-link mid-point voltage fluctuations can be reduced and the loss distribution can be made more uniform. This strategy is also called 60° flat-top SVM.

In order to obtain the maximum benefit of clamping, the 60° subintervals should be centered around the current peaks in the positive and negative half cycles [18]. This strategy is termed as the Switching-Loss-Minimized SVM (SLM-SVM) in this work. The benefits of SLM-SVM can be fully exploited for the phase a current angle ϕ in the range of $-30° \leqslant \phi \leqslant 30°$ which corresponds to the power factor (PF) in range of 0.86 leading $\leqslant PF \leqslant 0.86$ lagging.

III. Implementation of Switching-Loss-Minimized Space Vector Modulation (SLM-SVM)

SLM-SVM can be implemented using a look-up table or using a space phasor machine [20]. In either of the approaches, the switching sequences for each of the four regions (Figure 3) in the six sectors are stored in memory. Depending on the sector and the region in which $V_{\rm ref}$ is located, the corresponding sequences are retrieved from memory. In the first approach, the switching times for each vector for different locations of $V_{\rm ref}$ are also stored in memory in the form of look-up tables. This requires minimum computation effort and is easily implemented on a general purpose DSP. In the latter approach, the switching times are computed online for each of the sampled values of $V_{\rm ref}$. This approach is computation intensive and needs a sophisticated processor [20].

The sequence of states depends upon the position of the 60° clamping window. For fixed clamping-window positions like in [14], it is required to store one sequence. But, complications arise while implementing the SLM-SVM in which the clamping window changes dynamically depending on the power factor angle as it would require several conditional statements to choose from different switching sequences. In order to overcome this tedious decision-making process, a general algorithm for implementation of SLM-SVM is proposed in this work. The implementation is independent of the position of the clamping window. With a little modification to ensure equal times for positive and negative clamping in one fundamental period, the width of the clamping window can also be adjusted to implement, for example, 30° or 15° clamping strategies and would be presented in a future publication. This implementation is particularly useful for experimental purposes when the various modulation schemes have to be compared and evaluated against each.

A. State Matrix Representation

This implementation of SLM-SVM arranges all of the space vectors in the form of three three-dimensional matrices,

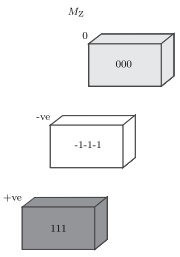


Figure 5: The M_Z matrix for SLM-SVM

TABLE II: Contents of M_Z

Element	Contents	
$M_Z[0]$	V_{0+}	(111)
$M_Z[1]$	V_{0-}	(-1-1-1)
$M_Z[2]$	V_0	(000)

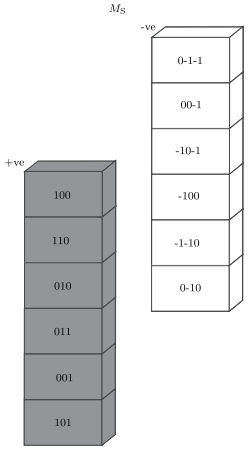


Figure 6: The M_S matrix for SLM-SVM

TABLE III: Contents of M_S

Element	Contents	
$M_S[0][0]$	V_{1+}	(100)
$M_S[1][0]$	V_{2+}	(110)
$M_S[2][0]$	V_{3+}	(010)
$M_S[3][0]$	V_{4+}	(011)
$M_S[4][0]$	V_{5+}	(001)
$M_S[5][0]$	V_{6+}	(101)
$M_S[0][1]$	V_{1-}	(0-1-1)
$M_S[1][1]$	V_{2-}	(00-1)
$M_S[2][1]$	V_{3-}	(-10-1)
$M_S[3][1]$	V_{4-}	(-100)
$M_S[4][1]$	V_{5-}	(-1-10)
$M_S[5][1]$	V_{6-}	(0-10)

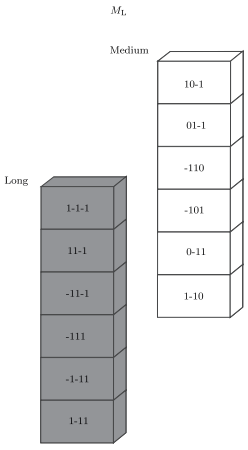


Figure 7: The M_L matrix for SLM-SVM

TABLE IV: Contents of M_L

Element	Contents	
$M_L[0][0]$	V_7	(1-1-1)
$M_L[1][0]$	V_9	(11-1)
$M_L[2][0]$	V_{11}	(-11-1)
$M_L[3][0]$	V_{13}	(-111)
$M_L[4][0]$	V_{15}	(-1-11)
$M_L[5][0]$	V_{17}	(1-11)
$M_L[0][1]$	V_8	(10-1)
$M_L[1][1]$	V_{10}	(01-1)
$M_L[2][1]$	V_{12}	(-110)
$M_L[3][1]$	V_{14}	(-101)
$M_L[4][1]$	V_{16}	(0-11)
$M_L[5][1]$	V_{18}	(1-10)

namely M_Z, M_S and M_L as shown in Figure 4. M_Z contains the three zero states as shown in Figure 5. It has one row, three columns and three layers. The three columns contain the switching states for each of the phase legs respectively. The first layer corresponding to the index 0 (according to indexing terminology of C language) contains the positive clamping state (111). The next layer, with the index of 1 corresponds to the negative clamping state given by (-1-1-1). The last layer with an index of 2 has the zero clamping state (000). This is summarized in the table II.

The matrix M_S contains the states pertaining to the vertices of the inner hexagon in Figure 2. The sectors are represented in the rows of M_S and the redundant states are contained in the layers as shown in Figure 6. The sign $+$ or $-$ indicates whether a phase can be clamped to positive or negative dc bus voltage. This is summarized in the table III.

The matrix M_L contains the states pertaining to the vectors of the outer hexagon in Figure 2. The outer hexagon has 12 vectors without any redundancy. As with M_S, the sector information is represented in the rows. The first layer contains the long vectors and second layer contains the medium vectors as shown in Figure 7.

B. Derivation of the Formulae

In order to derive the formula for the state selection, the case where V_{ref} is located in region 1 of sector 1 as shown in Figure 3 is considered. The chosen states would be V_{0+}, V_{2+} and V_{1+}. The switching sequences for positive and negative clamping in region 1 of all sectors is shown in table V.

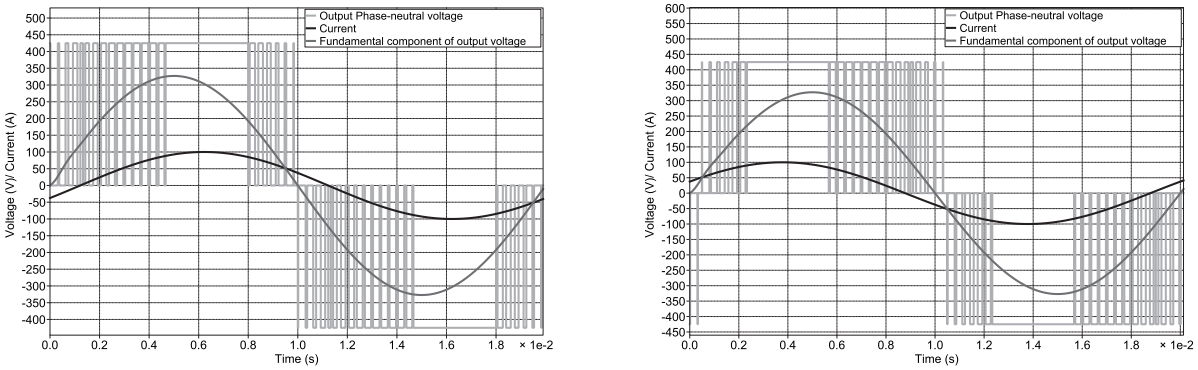
Looking at the positive-clamping sequences, the following observations can be made:

- The sequence always begins with V_{0+}.
- The second vectors in the sequences have even subscripts.
- The third vectors in the sequences have odd subscripts.
- For every even-numbered sector, the second vector of the sequence has the same subscript as the sector number and the third vector of the sequence has its subscript incremented by one. For sector 6, the subscript of third vector in sequence is obtained by 'wrapping-around' to 1 since sector 7 does not exist.
- For every odd-numbered sector, the third vector of the sequence has the same subscript as the sector number and the second vector of the sequence has its subscript incremented by one.

Similar symmetries can be observed in the negative-clamping sequences as well. In order to describe the general-

TABLE V: Positive and negative clamping sequences in the region 1

Sector	Positive clamping sequence
1	$V_{0+} \rightarrow V_{2+} \rightarrow V_{1+} \rightarrow V_{2+} \rightarrow V_{0+}$
2	$V_{0+} \rightarrow V_{2+} \rightarrow V_{3+} \rightarrow V_{2+} \rightarrow V_{0+}$
3	$V_{0+} \rightarrow V_{4+} \rightarrow V_{3+} \rightarrow V_{4+} \rightarrow V_{0+}$
4	$V_{0+} \rightarrow V_{4+} \rightarrow V_{5+} \rightarrow V_{4+} \rightarrow V_{0+}$
5	$V_{0+} \rightarrow V_{6+} \rightarrow V_{5+} \rightarrow V_{6+} \rightarrow V_{0+}$
6	$V_{0+} \rightarrow V_{6+} \rightarrow V_{1+} \rightarrow V_{6+} \rightarrow V_{0+}$
Sector	Negative clamping sequence
1	$V_{0-} \rightarrow V_{1-} \rightarrow V_{2-} \rightarrow V_{1-} \rightarrow V_{0-}$
2	$V_{0-} \rightarrow V_{3-} \rightarrow V_{2-} \rightarrow V_{3-} \rightarrow V_{0-}$
3	$V_{0-} \rightarrow V_{3-} \rightarrow V_{4-} \rightarrow V_{3-} \rightarrow V_{0-}$
4	$V_{0-} \rightarrow V_{5-} \rightarrow V_{4-} \rightarrow V_{5-} \rightarrow V_{0-}$
5	$V_{0-} \rightarrow V_{5-} \rightarrow V_{6-} \rightarrow V_{5-} \rightarrow V_{0-}$
6	$V_{0-} \rightarrow V_{1-} \rightarrow V_{6-} \rightarrow V_{1-} \rightarrow V_{0-}$



(a) Output waveforms for SLM-SVM at $\phi = 22°$ lagging

(b) Output waveforms for SLM-SVM at $\phi = 22°$ leading

Figure 8: Working principle of SLM-SVM

ized algorithm, the following variables are defined:

- $sector$ is a variable which indicates the sector in which V_{ref} is located. The SVM diagram of Figure 2 can be divided into six sectors. So, $1 \leq sector \leq 6$.
- $clamping$ is a boolean variable that indicates the nature of clamping and $clamping \in \{0, 1\}$. The value of 0 indicates clamping to the positive dc voltage and 1 to the negative voltage.
- $condition$ is a boolean variable given by:

$$condition = \mathrm{isodd}(sector) \oplus clamping \tag{3}$$

where 'isodd' is a conditional statement which returns a value of 1 if $sector$ is odd, and 0 if $sector$ is even and $\oplus$ is the XOR binary logical operator for two bits.

The switching sequence for region 1 can now be represented in terms of the contents of the three matrices using the following formula:

Region-1:

$$M_{\mathrm{Z}}[clamping] \leftrightarrow M_{\mathrm{S}}[sector - 1 + condition][clamping] \leftrightarrow M_{\mathrm{S}}[sector - 1 + !condition][clamping] \tag{4}$$

where ! indicates the unary negation operator (NOT), $\leftrightarrow$ indicates that the sequence repeats in reverse order in one switching cycle. The indices x and y in, for example, $M_{\mathrm{S}}[x][y]$ indicate the number of row and layer respectively in the M_{S} array where the switching state to be employed is located in the form of a string. Similarly, the switching sequences for the other three regions can be expressed as follows.

Region-2:

$$M_{\mathrm{S}}[sector - 1 + condition][clamping] \leftrightarrow M_{\mathrm{S}}[sector - 1 + !condition][clamping] \leftrightarrow M_{\mathrm{L}}[sector - 1][1] \tag{5}$$

Region-3:

$$M_{\mathrm{S}}[sector][clamping] \leftrightarrow M_{\mathrm{L}}[sector - 1 + condition][!clamping] \leftrightarrow M_{\mathrm{L}}[sector - 1 + !condition][condition] \tag{6}$$

Region-4:

$$M_{\mathrm{S}}[sector - 1][clamping] \leftrightarrow M_{\mathrm{L}}[sector - 1][condition] \leftrightarrow M_{\mathrm{L}}[sector - 1][!condition] \tag{7}$$

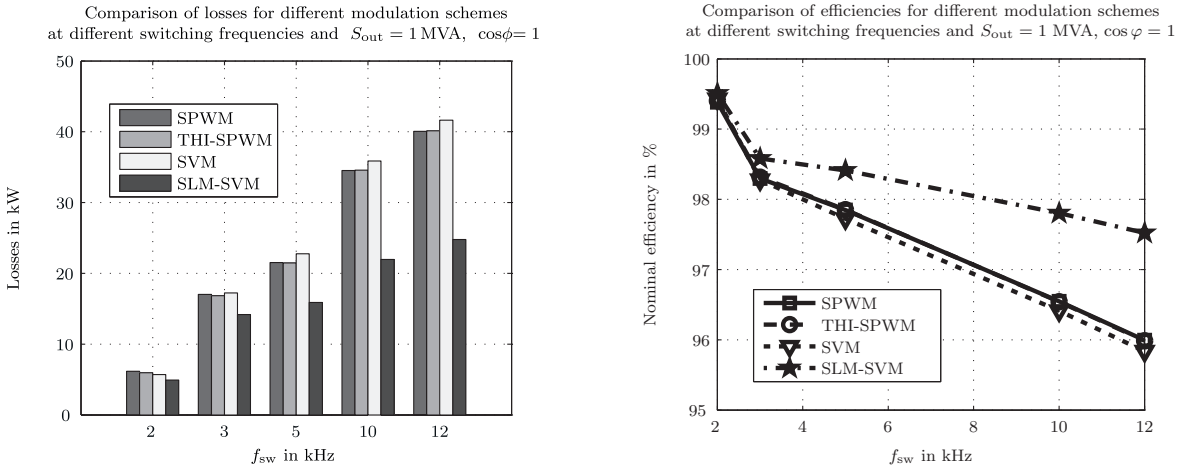
These formulae are applicable to all sectors since each of them can be split into such four triangular regions. Thus, it is possible to represent all the vectors in the space-vector diagram in the form of the three matrices. The only additional calculation involved in SLM-SVM as compared to the traditional implementation of SVM is the determination of the value of the variable $condition$ which is only a binary operation and is determined in one instruction cycle of the controller. The switching states are still read from the memory as in the case of the traditional implementation. However, the switching sequences are generated through (4)-(7) and the switching times are calculated on-line. The clamping is automatically taken care of by merely changing the value of the $clamping$ variable. Thus, these formulae enable on-line switching-sequence generation depending upon the current power factor angle.

IV. Simulation Results

In this work, a 1 MVA TNPC converter of Figure 1 was simulated using Matlab and Plecs. The dc-bus voltage U_{dc} is taken as 850 V with the nominal output line-line voltage of 400 V. The devices used for the loss calculations are the FZ3600R12HP4 IGBTs from Infineon. An *LCL* filter with damping resistor of $0.2\,\Omega$ is used to comply with the grid requirements on the output side. The other filter parameters are $L_{\mathrm{inv}} = 68\,\mu\mathrm{H}$, $C_{\mathrm{f}} = 597\,\mu\mathrm{F}$ and $L_{\mathrm{grid}} = 26\,\mu\mathrm{H}$.

Figure 8a and 8b depict the working of the SLM-SVM algorithm. In this figure, the waveforms for two different power factor angles, namely, $\phi = 22°$ lagging and $\phi = 22°$ leading are presented. Only the fundamental component of the current is shown. The fundamental component of the phase voltage is also shown for reference. It can be seen that the algorithm works well and the 60°-clamping window is centered around the current peak as long as the power factor angle is in the range $-30° \leq \phi \leq 30°$. Beyond this range, the clamping window cannot center itself around the current peak resulting in only a partial reduction in the switching losses as compared to standard SVM.

Figures 9a and 9b depict a comparison of the total losses and the efficiencies, respectively, for the four modulation schemes



(a) Total losses at different switching frequencies

(b) System efficiencies at different switching frequencies

Figure 9: Comparison of total losses and the system efficiencies for different modulation schemes

at different switching frequencies. As the SLM-SVM strategy effectively reduces the switching losses by at least 33 %, the reduction in losses becomes more prominent at higher frequencies. Moreover, the decrease in efficiency is also not that steep with increasing switching frequency.

V. Conclusion

SPWM, THI-SPWM, SVM and SLM-SVM were discussed and compared in this paper. It is found that the use of SLM-SVM results in lower total converter losses and higher efficiency. The switching frequency can be increased correspondingly to decrease the size of passive filter elements. A generalized algorithm is developed to implement SLM-SVM without the need to store individual switching sequences. The highlight of this algorithm is that the clamping window and clamping position can be dynamically adjusted to incorporate inductive as well as capacitive loads. The algorithm is developed for TNPC but is equally applicable to standard NPC converters as well.

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