Coreless Planar Transformer for Hard-Switching Applications

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Kurzfassung

Leistungshalbleiter werden meist in schaltenden Anwendungen eingesetzt. Hartes Schalten ist hierfür ein gängiges und einfaches Funktionsprinzip, insbesondere bei induktiven Lasten. Der Schaltvorgang ist gekennzeichnet durch eine signifikante Überlappung zwischen Spannung und Strom. Diese Überlappung erwärmt den Halbleiter und erzeugt Verluste, da die entsprechende Energie nicht an die Last übertragen wird. Diese Schaltverluste sind erheblich und ein limitierender Faktor für die Schaltfrequenz von hart schaltenden Anwendungen. Durch Verkürzung der Übergangsdauer können die Schaltverluste reduziert werden. Die Nachteile schnellerer Übergänge in hart schaltenden Anwendungen sind in der Regel höhere Überschwingungen und außerdem die Erzeugung von elektromagnetischen Störungen. Überspannungen beim Ausschalten müssen bei der Wahl der notwendigen Durchbruchspannung des Halbleiters berücksichtigt werden und können so den Wirkungsgrad weiter reduzieren. Da die Durchbruchspannung mit dem Durchlasswiderstand des Halbleiters korreliert, werden die Leitverluste indirekt beeinflusst. Daher wird die maximale Überspannung oft begrenzt. Ein gängiger Ansatz zur Reduzierung der Überspannungen für einen Leistungshalbleiter ist die Minimierung der Induktivität im Kommutierungspfad. Ein in Reihe mit den Leistungsanschlüssen des Halbleiters geschalteter Transformator kann jedoch für verschiedene Anwendungen von Vorteil sein. Insbesondere die hohen Stromgradienten bei schnellen, harten Schaltvorgängen sorgt für eine hohe, und somit gut nutzbare Ausgangsspannung des Transformators. Dennoch muss die Induktivität der in Reihe mit dem Halbleiter geschalteten Transformator-Wicklung minimal gehalten werden. In dieser Arbeit wird ein neues Design eines kernlosen Planartransformators vorgestellt. Eine hohe magnetische Kopplung und ein einstellbares Übersetzungsverhältnis sowie eine besonders hohe Bandbreite sorgen dafür, dass die Induktivität in Reihe mit dem Halbleiter minimal gehalten werden kann. Der zweischichtige Aufbau ist zudem für verschiedene Substrate, insbesondere Leiterplatten, geeignet. Ein bis zur ersten Resonanzfrequenz gültiges Simulationsmodell des neuen Übertragerdesigns wird erstellt und verifiziert. Die Anwendung, für die der Übertrager in dieser Arbeit hauptsächlich eingesetzt wird, ist das induktive Feed-Forward Verfahren. Diese Methode zur Steuerung von Leistungshalbleitern beschleunigt das Umschalten in hart schaltenden Anwendungen. Die Methode wird analysiert und Verbesserungen für eine Auswahl von Leistungshalbleiter-Designs werden vorgeschlagen und verifiziert. Weiterhin wird die Ansteuerungsmethode modifiziert, um symmetrische Stromgradienten in parallel

geschalteten Leistungshalbleitern zu erreichen. Außerdem wird der Übertrager vergleichbar zu einer Rogowski-Spule als Stromsensor genutzt, um die hohen Stromgradienten beim Schalten zu charakterisieren. In der letzten in dieser Arbeit vorgestellten Anwendung wird der Übertrager zur Erzeugung einer isolierten Versorgungsspannung für die Gate Ansteuerung eingesetzt. Die Anwendung ist besonders vorteilhaft, wenn eine negative Versorgungsspannung erforderlich ist, z.B. aufgrund einer niedrigen Schwellspannung.

Abstract

Power semiconductors are mostly used in switching applications. Hard switching is a common and simple operation principle, especially for inductive loads. It is characterized by a significant overlap between voltage and current during the transition. This overlap heats up the semiconductor, wasting the energy since it is not transferred to the load. These switching losses are substantial and a limiting factor for the switching frequency of hard-switching applications. By decreasing the transition time, the switching losses can be reduced. The drawbacks of faster transitions in hard-switching applications are usually an increased ringing as well as the generation of electromagnetic interference. Especially the ringing further influences the efficiency. The voltage overshoot during turn off has to be taken into account when choosing the necessary breakdown voltage of the semiconductor. Since the breakdown voltage correlates with the on-state resistance of the semiconductor, the conduction losses are affected indirectly. Therefore, the maximum voltage overshoot is often restricted. A common approach to reduce the voltage overshoot for a given semiconductor is to minimize the inductance in the commutation loop. However, a transformer added in series with the power connectors of the semiconductor can be beneficial for various applications. Especially the high current gradients of fast switching transitions ensure a sufficient output voltage of the transformer. Still, the inductance of the transformer winding connected in series with the semiconductor has to be kept minimal. A new design of a coreless planar transformer is introduced in this work. A high magnetic coupling and an adjustable transformation ratio as well as a particularly high bandwidth ensure that the inductance in series with the semiconductor can be kept minimal. Furthermore, the two-layer design is suitable for various substrates, especially printed circuit boards. A simulation model of the new transformer design valid up to the first resonance frequency is created and verified. The application the transformer is mainly used for during this work is the inductive feed-forward method. This power semiconductor control method accelerates the transition in hard-switching applications. The method is analyzed and improvements for a selection of power semiconductor designs are suggested and verified. The driving method is also modified, to achieve symmetrical current gradients in parallel-connected power semiconductors. In addition, the transformer is used similar to a Rogowski coil in a current sensor to characterize the high current gradients during switching. In the final application presented in this work, the transformer is used to generate an isolated bias voltage.

Contents

1 Introduction

Despite the fact that the global corona pandemic lowered energy usage by 4 % in 2020, the 2019 level was already surpassed by 0.6 % in 2021 [1]. This continues the steady rise that began before the pandemic [2]. Power semiconductors account for a large proportion of the losses in motor drivers and also in switched-mode power supplies. Therefore, increasing the efficiency of power semiconductors on a continuous basis is critical to counteract the rising energy demand. The largest share of the 17.5 B$ market for power semiconductors is taken by the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET) with 45 %, followed by the insulated-gate bipolar transistor (IGBT) with 22 % [3]. Only a very small market share (< 4 %) is currently occupied by wide bandgap devices, but the share should increase in the future [4, 5]. The wide bandgap materials used for power semiconductors are mainly gallium nitride (GaN) and silicon carbide (SiC) at the moment. They offer lower conduction and dynamic losses as well as better thermal behavior [6].

The trend in the automotive industry towards electric vehicles is currently one of the biggest driver of the power electronics industry. The automotive market is believed to increase from around 1.5 B$ in 2020 to over 5.5 B$ in 2026 [7]. Even though initially IGBT devices will benefit from this growth, MOSFET offer advantages for the traction inverter of electric vehicles. Since electric motors usually are inductive loads, the traction inverter operate the power semiconductor in hard-switching mode. Since the MOSFET does not store a charge during turn on, the switching losses are significantly lower compared to an IGBT. In addition, the MOSFET may also have advantages in conduction losses. IGBTs are bipolar devices which means that an initial voltage drop is necessary to achieve a current through the junction of the different doping areas. This build-in voltage is around 0.7 V for Si devices. A MOSFET on the other side as a unipolar device has an almost linear output characteristic and thus offers a potential to reduce the losses in light-load or partial-load operation [8, 9]. Depending on the load distribution during the drive cycle, with SiC MOSFETs a 3-5 % higher efficiency is expected compared to Si IGBTs [10, 11]. Since this energy saving can directly be transferred into a higher mileage of the vehicle, this is an appealing selling point in the current race for the highest range. It is expected that SiC MOSFET due to this reason will occupy a significant share of the emerging market for traction inverters [4].

As mentioned earlier, traction inverters are typically operated in hard-switching mode. Hard switching is characterized by a significant overlap between voltage and current during the transition. Thus, faster transitions of the power semiconductor reduce the losses and can thereby safe energy. An alternative is soft switching where either current or voltage is brought to zero before the transition to reduce the switching losses of the power semiconductor [12, 13]. However, the implementation can be difficult, especially if a high load range is required [14]. For this reason the focus of this work is on hard switching and it is a general condition for all design optimizations of this work. Another application which can be operated in hard-switching mode and benefits from lower dynamic losses are switched-mode power supplies. Here, the reduction of the losses can either shrink the cooling attachments or is used to achieve higher switching frequencies. With higher switching frequencies, often the size of passive components can be reduced [15]. Both approaches increase the power density which is an important characteristic for switched-mode power supplies.

There are several approaches to reduce the dynamic losses in hard-switching applications: The semiconductor, the assembly and interconnection technology (AIT), or the control can be optimized. As mentioned earlier, wide bandgap materials are one option to reduce the dynamic losses. Furthermore, conventional Si MOSFETs are also still improved [16]. The current gradients during switching transition result in a voltage drop over the inductances of the AIT. Reducing these inductances can prevent or reduce an over voltage during turn off [17] and thereby reduce the necessary blocking voltage of the power semiconductor. Moreover, the current gradient can be increased, reducing the switching duration and thereby the dynamic losses.

To control the power semiconductors, either current-source, voltage-source or resonant gate driver are used [18]. For voltage and current controlled power semiconductor designs, the device is turned on above a specific threshold voltage and stays off if the gate voltage is below this threshold. Furthermore, the switching duration depends on the gate driver and its ability to shift the gate voltage between on and off state. A high gate current during transition can reduce the switching duration and thereby the dynamic losses in hard-switching applications. Current-source gate driver offer an almost fixed gate current up to a predefined voltage limit, for example by using an inductance in combination with a full bridge or a current mirror [19]. An inductance in the gate loop can also be used to realize a resonant gate driver to improve the gate driver efficiency. However, a high inductance in series with the gate can slow down the transition [20] by decreasing the average gate current and thereby increases the dynamic losses in hard-switching applications. Conventional voltage-source gate driver use a resistor in series with the gate to adjust the gate current. A half bridge is used to switch between the bias voltages of the gate driver. To temporarily increase the gate current, a capacity in parallel to the gate resistor [21, 22] or another boost circuits [23] can

reduce the initial impedance. If the current should be increased further, a higher bias voltage can be applied [22, 24]. The bias voltage can also be increased by inducing an additional voltage into an inductance in series to the gate, for example by a magnetic field created by the source current [25]. This method will be called inductive feed forward (IFF) and is a main focus of this work.

However, faster transitions in hard-switching traction inverters and switched-mode power supplies also enhance electromagnetic interference (EMI) [26, 27]. Through slope shaping, the electromagnetic emissions can be reduced while still accelerating the transition [28, 29]. An active current-source gate driver can provide an optimized gate current during transition to influence the shape of the voltage and current transitions [30]. For voltage-source gate drivers, switchable gate resistors can be used to control the transition [31]. Overall, accelerating the switching is not always beneficial and slowing down the transitions of modern semiconductors can also be desired at certain operation points. In traction inverters, fast transitions can have negative impacts on the electric motor. The high slew rate can damage the bearings because of displacement currents between rotor and stator [32]. In addition, partial discharge between the motor windings can damage the isolation [33].

1.1 Scope of this thesis

This work focuses on Si MOSFETs due to their dominance in the power semiconductor market. Wide bandgap devices are also considered, because of the increasing significance as well as market share. Improvements for these devices could have a broad impact in various applications, for example traction inverters or switched-mode power supplies. The overall objective is to reduce the dynamic losses to increase the efficiency especially for high switching frequencies. This is achieved by applying the IFF method which temporarily increases the voltage applied to the gate terminal of a power semiconductor. Through a transformer which utilizes the steep current gradients of hard-switched applications in the primary winding, a voltage is induced to the secondary winding which is connected in series to the gate (cf. figure 3.4).

The basics of the IFF method were developed by Michael Ebli for his Ph.D. dissertation [34]. To realize the transformer of the IFF method, he applied a four-layer transformer design to a printed circuit board (PCB). Furthermore, separate gate connections are used for turn on and turn off. This is because the work concentrates on the reduction of the turn-on losses. It is shown that voltage controlled SiC [25], GaN [35] as well as Si [36] devices can benefit from the method.

Due to this work, it will be possible to use the IFF method even with only a single gate connection. To achieve this, emphasis is placed on the design and impact of the transformer. An accurate model of the transformer is created to assess the influence on the dynamic losses and identify critical elements. Due to the high bandwidth of a new two layer design, the impact of the transformer on the circuit is minimized. Thereby, oscillations can be mitigated and also the dynamic losses can be reduced further. Several improvements and additional benefits of the IFF method will be shown and explained but also the impact on the EMI will be analyzed. Effects of the fast transitions on external components beyond the EMI were not evaluated.

In addition to the IFF method, further functionalities can benefit from the new transformer design. In this work it will be used to realize a current measurement with a high bandwidth. Moreover, a new approach to create a negative bias voltage in hard-switched applications will be introduced.

1.2 Outline of this thesis

In chapter 2 some initial considerations are laid out. The chapter starts with an introducing of a basic equivalent circuit for the utilized power semiconductors. A selection of semiconductor designs which have been considered are presented and compared by means of the elements in this equivalent circuit. The superjunction metal–oxide–semiconductor field-effect transistor (SJMOSFET) is chosen as the design which can benefit significant from the IFF method. Furthermore, the modeling methods used in this work are introduced and classified. The focus is the modeling and extraction of the parasitic elements added by the AIT. The work flow which is used to achieve a lumped element model is explained and limitations are clarified.

In chapter 3 the IFF method and associated with it the characteristics of hard switching are explained. The double pulse setup and a suitable simulation schematic are introduced as a tool to identify the switching losses. Based on simulation results with a SJMOSFET, the IFF method is compared to a conventional gate driving approach and the switching characteristics are depicted. Important model characteristics which have a considerable influence are listed and explained.

The novel design of a coreless planar transformer is introduced in chapter 4. First an appropriate lumped element model is established and a simple equation to estimate the first resonance frequency is suggested. The coupling capacitance is identified as a critical element to achieve a wide bandwidth. Based on a sensitivity analysis design recommendations are given for various design parameters of the transformer. The design is optimized for the requirements of the IFF method. The novel design is furthermore compared to a reference transformer used for the IFF method in preceding work. A PCB realization of the novel design is characterized and the measurement results compared to the simulation. The initial model is also extended to cover the effects of occurring eddy currents up to the first resonance frequency.

To determine the switching losses of the IFF method a suitable current measurement is necessary. In chapter 5 the new design of a coreless planar transformer is used similar to a Rogowski coil to realize a current sensor. An appropriate design and signal conditioning circuit are combined to realize an isolated current measurement with a sufficient bandwidth.

In chapter 6 further insides into the IFF method as well as variations of the method are presented. First, corresponding to the previous simulations, the new transformer design is combined with a SJMOSFET and the switching characteristics are measured and compared to a conventional gate driving approach. Furthermore, extensions to the IFF method are established. An additional freewheeling diode can ensure the safe turn off for power semiconductor with a low threshold voltage.

A rectifier can also be necessary for particular power semiconductor designs if a robust turn on with the IFF method should be achieved. In this chapter, the influence of the IFF method on the EMI is also examined. Measurements of a boost converter are compared which can be switched between the IFF method and a conventional gate driving approach by removing the coreless transformer. Moreover, the influence of the IFF method on parallel connected power semiconductors is analyzed. A cross coupled approach is suggested to balance the current during turn on. The last section shows the limitation of a coreless inductor by using the IFF method on an IGBT. In addition, the negative inductive feed forward (NIFF) is introduced, an approach in which the polarity of the inductor is inverted to limit the voltage during switching and thereby slow down the transition to reduce the EMI.

Another application which can benefit from the new design of a coreless planar transformer is presented in chapter 7. The target is to create a negative bias voltage to ensure a safe turn off during high slew rates. A suitable circuit as well as measurements of an example setup are presented in this chapter. The application is particularly advantageous if the semiconductor features a low threshold voltage.

In chapter 8 the results of this work are summarized and an outlook is given to reveal possible improvements and starting points for further investigations.

2 Critical semiconductor model elements and applied modeling methods

To evaluate what influence the design of a power semiconductor has on the switching characteristics, a basic equivalent circuit is necessary. In figure 2.1 a simple approach is shown which consists of the major reactances. In addition, a current source is chosen to represent the operating point of the semiconductor. Because the focus is on the switching, the resistances are neglected. Due to these simplifications, the model is suitable for comparing various power semiconductors. Some parts are grayed out, for example the gate source diode D_{GS} or the Kelvin contact (K), since these are only applicable for individual power semiconductor designs or packages but necessary for a sufficient electric description of these.

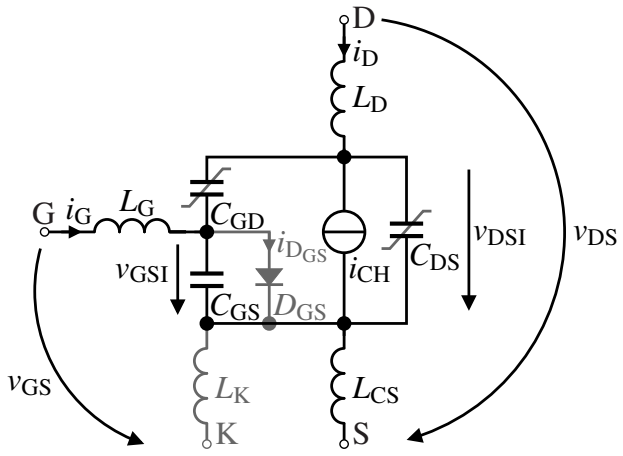


Fig. 2.1: Basic equivalent circuit used throughout this work for power semiconductors.

The depicted capacitances have a significant influence on the transition performance of the power semiconductor. Due to a simpler electrical characterization, the capacitances are often specified as follows [37]:

$$C_{RSS} = C_{GD}, \qquad C_{ISS} = C_{GS} + C_{GD}, \qquad C_{OSS} = C_{DS} + C_{GD}. \tag{2.1}$$

Especially if the drain connection (D) of the device is the switching potential, the output capacitance C_{OSS} has a significant influence on the efficiency. Since the corresponding capacitances have

to be charged or discharged, the transition is extended for a higher C_{OSS} if the power semiconductor design stays the same.

Furthermore, the inductances of the device result in additional voltage drops during current transitions. In the case of discrete power semiconductors, any bond wires and other package interconnects increase the corresponding parasitic inductance. Some devices offer an additional Kelvin contact to minimize the critical common source inductance L_{CS}. A separate inductance of the Kelvin connection L_{K} is added in parallel with as suggested in [38]. A leadless package is another commercially available solutions to reduce the inductances L_{CS}. During current transitions the additional voltage drops over the parasitic inductances reduce the gate-source voltage v_{GS} and the drain-source voltage v_{DS}. For rapid transitions especially the above mentioned parasitic reactances strongly affect the resulting internal gate-source voltage v_{GSI} and the internal drain-source voltage v_{DSI}. For field-effect transistor designs this also effects the channel current i_{CH}, since it is mainly defined by these two voltages:

$$i_{\mathrm{CH}}(t) = f(v_{\mathrm{GSI}}(t), v_{\mathrm{DSI}}(t)). \tag{2.2}$$

This work also uses current controlled devices. For the particular design an additional diode between the gate and the source can be used to model the behavior [39]. Above the threshold voltage V_{th} a current through D_{GS} forms the electron channel and thereby controls i_{CH}:

$$i_{\mathrm{CH}}(t) = f(i_{\mathrm{D_{GS}}}(t), v_{\mathrm{DSI}}(t)) \quad \text{if} \quad v_{\mathrm{GSI}} > V_{\mathrm{th}}. \tag{2.3}$$

The transition characteristics for both, voltage and current controlled, devices are strongly affected by the reactances, due to the dependencies in equation 2.2 and equation 2.3. Independent of the control mechanism, a steady on state is attained after the turn-on transition. At this operation point, the gate current i_{G} as well as v_{GS} do not change anymore. In the ideal equivalent circuit, there is no voltage drop over the inductances and no current through the capacitances. The drain current i_{D} matches channel current i_{CH} and the on-state resistance R_{DSon} of the device can be determined without taking the reactances into account:

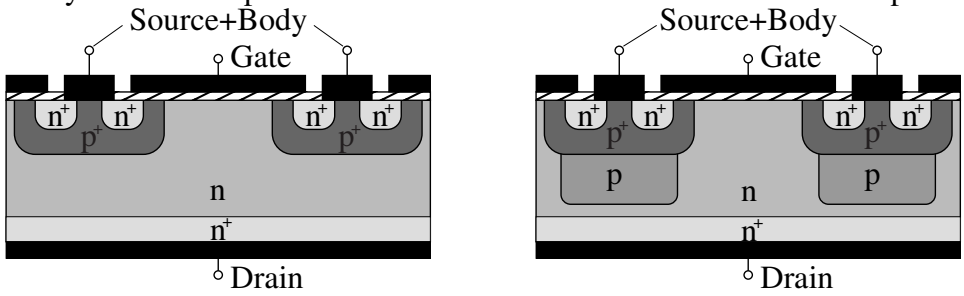
$$R_{\mathrm{DSon}} = \frac{v_{\mathrm{DS}}}{i_{\mathrm{D}}} \quad \text{with} \quad v_{\mathrm{GS}} = \text{const} \quad \text{and} \quad i_{\mathrm{G}} = \text{const}. \tag{2.4}$$

Overall, the reactances have a significant influence on the switching characteristics but do not influence the static turn-on behavior. Thus, focusing on these elements is only important for fast transitions. However, especially the capacitances can correlate with the on resistance. Choosing an appropriate power semiconductor design is therefore also crucial for fast and efficient transitions.

2.1 Power semiconductor evaluation

A benchmark for all power semiconductor designs is the feasible on-state resistance R_{DSon} per area for a necessary blocking voltage. Furthermore, the dynamic losses have become more and more important in recent years. In hard-switching applications, switching losses are reduced by the faster voltage transitions that can be achieved by improved semiconductors, especially wide bandgap devices. This chapter introduces several designs with the focus on minimizing the dynamic losses. Moreover, current commercially available implementations are compared on the basis of their characteristics to differentiate the designs.

Double-diffused metal-oxide semiconductor field-effect transistor (DMOSFET)
The basic structure of a conventional power MOSFET is the DMOSFET shown in figure 2.2(a). The polysilicon gate is isolated from the semiconductor by a thin layer of silicon dioxide (SiO_2) outlined by the cross-hatching. Once the gate voltage exceeds the threshold voltage, an n-type conductive channel is formed below the oxide in the p^+-region. A vertical load current during on-state is realized by placing the source on the top and the drain on the bottom side of the wafer. The breakdown voltage can be defined by the thickness and doping of the n-region. Due to the higher doping level of the p^+-base layer, the depletion layer extends primarily into the n-drift region. An advantage of this design is that the influence of the channel resistance on the overall on-resistance is reduced with increasing breakdown voltage and mainly dependent on the doping of the n-region. The theoretically achievable specific on-resistance of a DMOSFET can thus be specified.



(a) DMOSFET (b) SJMOSFET

Fig. 2.2: Basic cross sections of selected Si power semiconductor designs.

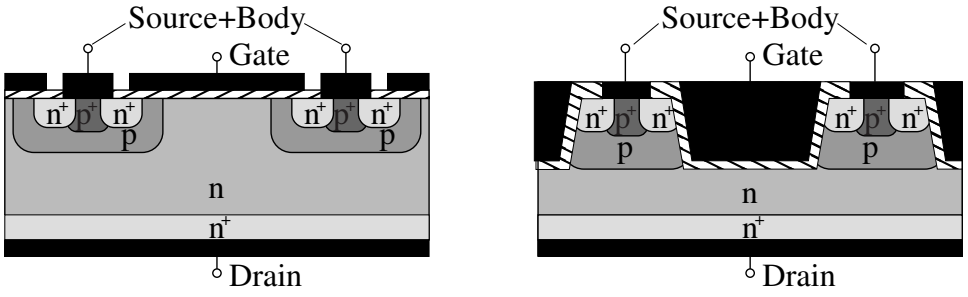
Superjunction metal–oxide–semiconductor field-effect transistor (SJMOSFET)
To achieve a lower on-resistance for high breakdown voltages, p-doped trenches have been added to the DMOSFET design to create the SJMOSFET in figure 2.2(b). Through that, the doping of the n-region can be increased, lowering the on-resistance. The additional p-doped trenches compensate the higher space charge to sustain the breakdown voltage. This additional layer also results in a hardly usable inverse diode [6].

Silicon carbide (SiC) and gallium nitride (GaN)

In recent years various designs utilizing SiC and GaN have been presented. Both materials differ from silicon in that they offer a higher band gap. A much lower intrinsic carrier concentration is achieved, which reduces the leakage current and increases the temperature range [40]. A high electric breakdown field allows for a reduction of the drift region for a given blocking voltage. The devices offer a significant lower specific on resistance and therefore a higher current density can be realized, leading to smaller devices with a lower gate charge. Thus, shorter transition times for a specific on-resistance are possible. However, wafers of both materials are still more expensive than silicon wafers [41].

SiC DMOSFET

SiC is especially suitable for high voltage DMOSFET implementations. A high saturation velocity adds to the shorter drift region and is the reason that especially with higher blocking voltages the specific on-resistance of SiC devices is increasing slower compared to Si devices [42]. However, the doping of the p^+-base layer of the Si DMOSFET in figure 2.2(a) has to be reduced to achieve a comparable lifetime to silicon devices at all temperatures. For SiC devices, a low channel resistance has to be balanced with a high dielectric reliability [43]. An additional p^+-region is necessary to connect the body diode and prevent the parasitic npn bipolar transistor from causing a secondary breakdown [44, p. 800]. The resulting cross section can be seen in figure 2.3(a). Since the forward voltage drop of the intrinsic body diode is higher in a SiC DMOSFET compared to a Si DMOSFET, additional measures can be necessary to limit the reverse conduction losses [45].



(a) SiC-DMOSFET (b) SiC-TMOSFET

Fig. 2.3: Basic cross sections of selected SiC power semiconductor designs.

SiC TMOSFET

Adding a trench for the gate has several improvements for a SiC-MOSFET. Since the gate oxide can be protected from high field strength, the channel resistance has not be balanced with a high dielectric reliability anymore [46]. The lower R_{DSon} can also be realized due to the higher possible channel mobility [47]. Overall, there is already multiple research on trench power semiconductors

[48]. A disadvantage is still the complex manufacturing process which is required to realize a homogeneous trench.

High-electron-mobility transistor (HEMT)

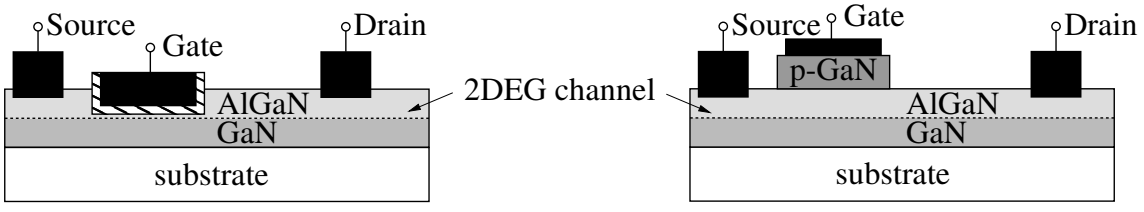
GaN power transistors can further reduce the on-resistance by an aluminum gallium nitride (AlGaN) layer which creates a heterostructure at the crystal boundary to a GaN layer. This increases the electron velocity due to a two-dimensional electron gas (2DEG) during on-state [49]. HEMTs take advantage of this effect and realize a lateral channel in the 2DEG. Various designs realizing normally off devices can be found [50].

Heterojunction field-effect transistor (HFET)

HEMTs which are controlled by the gate voltage are often referred to as HFETs. One way to implement a normally off design is by constantly depleting the 2DEG channel, for example, by reducing the aluminum mole fraction or the thickness of the AlGaN layer [51]. A possible realization with a recessed isolated gate is shown in figure 2.4(a) [52]. The downside to these designs is the low threshold voltage since reducing the electron density in the 2DEG of the transistor channel also reduces the on-resistance [53].

Gate injection transistor (GIT)

Another approach to achieve a normally off HEMT is to use an additional layer of a p-doped semiconductor beneath the gate to deplete the channel, see figure 2.4(b). Usually p-doped AlGaN or p-doped GaN layers are used [51, 53, 54]. If there is only a negligible gate current during turn-on, these devices are primarily controlled by the gate voltage and still referred to as HFETs [53]. For some designs the conductive channel in figure 2.4(b) is more reliant on the hole injection from the p-type gate. The on-state resistance is dependent on the gate current and the device is therefore referred to as a GIT [51]. In order to maintain the on-state, a continuous gate current is necessary.



(a) HFET (b) HFET/GIT

Fig. 2.4: Basic cross sections of selected GaN HEMTs.

2.1.1 Comparison of the considered semiconductor designs

A common DC link voltage for power electronics targeting domestic appliances, lighting, or consumer electronics, is 400 V. To cover these segments, 600 V or 650 V power devices are available from several suppliers. This voltage class is especially suitable for a comparison since implementation of most of the previously presented designs are available. The parasitic inductances of the discrete semiconductor, which are not the focus of this comparison, are mainly influenced by the packaging. Comparable packages are chosen whenever possible.

For conventional Si power semiconductors, SJMOSFETs are the common choice in this voltage domain. The selected 600 V devices [55–58] are optimized to reduce the dynamic losses while still offering a low R_{DSon} [59]. For SiC, implementations of both previously introduced designs are chosen: On the one hand, a 650 V DMOSFET [60] and, on the other hand, a 650 V TMOSFET [61–63]. The selected GaN implementations are both based on the design in figure 2.4(b). However, one is a 650 V HFET [64–67] and the other a 600 V GIT [68].

The characteristics of all implementations are determined at similar operating conditions to be able to compare the different designs. R_{DSon} is extracted from the datasheet for a junction temperature of 125 °C and a i_{D} of 20 A. Furthermore, R_{DSon} is used as the main reference for the comparison. In figure 2.5 the trend of C_{OSS} is shown for all considered designs. As described previously, C_{OSS} has a significant influence on the switching losses and should therefore be minimized. For the considered resistance range, the SJMOSFET offers the lowest C_{OSS}, at least for a v_{DS} of 400 V at which the capacitance is defined.

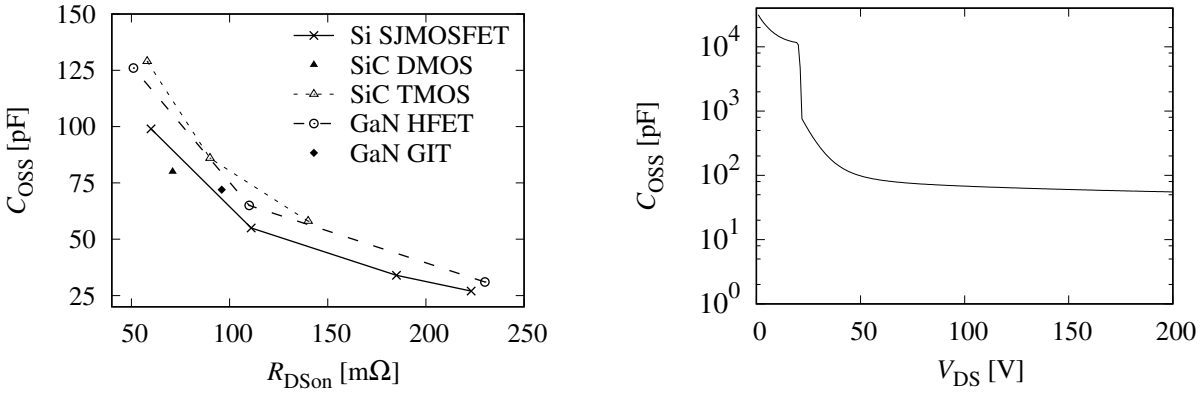


Fig. 2.5: Comparison of the output capacitance of selected technologies and the voltage dependency of C_{OSS} for a SJMOSFET.

The SJMOSFET is designed to offer a particularly low C_{OSS} at a high v_{DS}. This can be seen in the simulated C_{OSS} trend shown in the same figure 2.5 for up to 200V. In the voltage range below 50 V,

the output capacitance increases significantly. Since this voltage range is passed in every switching event, the implications of a low C_{OSS} resulting in lower switching losses are misleading. Therefore, the effective output capacitance $C_{\mathrm{O(ER)}}$ in figure 2.6 is more suitable to compare the effectiveness in hard-switching applications. $C_{\mathrm{O(ER)}}$ describes a fixed capacitance that provides the same stored energy as C_{OSS} while v_{DS} is rising from 0 to 400 V. Therefore, either the SiC implementations or the GaN GIT offers the lowest charge in combination with a low resistance if $C_{\mathrm{O(ER)}}$ is used for comparison.

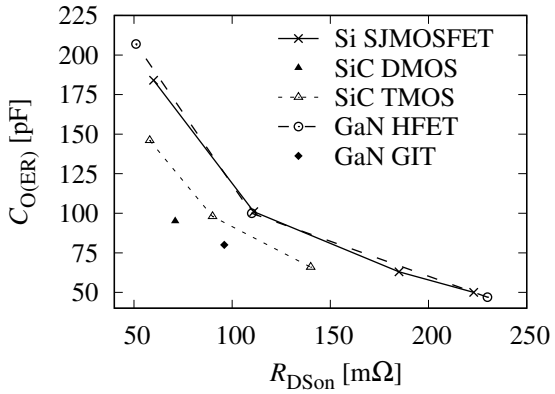


Fig. 2.6: Comparison of the effective output capacitance of selected technologies.

Another important characteristic, especially for fast transitions, is the gate-drain capacitance C_{GD}; see figure 2.7. If the drain is the switching potential, this capacitance slows down the transition due to the Miller effect. A low value results in a short Miller plateau and therefore in a fast transition. A more general characteristic effecting the transition duration is the necessary gate charge Q_{G}. This charge is necessary to switch the device to its R_{DSon} and thus a lower value can result in a faster transition. However, since the impact of the Miller effect is depending on the slew rates in the application, its impact on Q_{G} is excluded from the datasheet value. The GaN GIT achieves the lowest value for both characteristics. However, since above V_{th} it is a current-controlled device (e.g. equation 2.3), these characteristics are inconclusive. The values are only applicable up to the moment the diode D_{GS} (e.g. figure 2.1) is conducting.

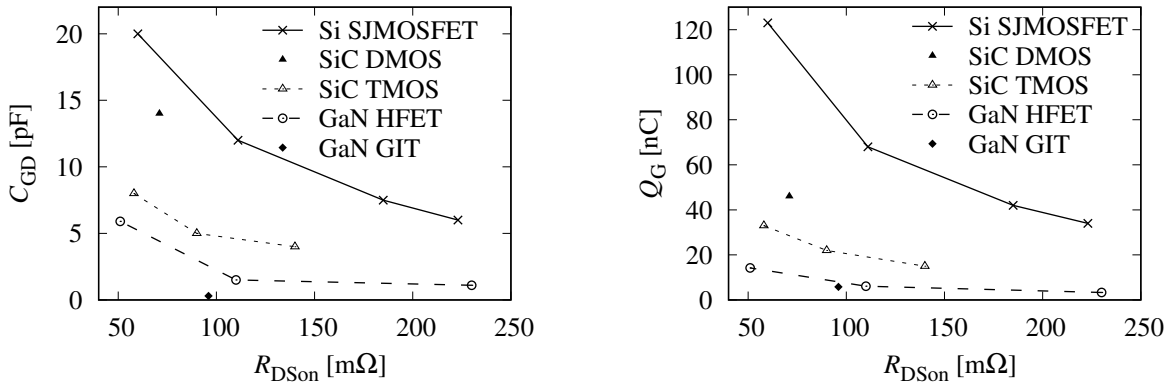


Fig. 2.7: Gate-drain capacitance and necessary gate charge of selected technologies.

Overall, the SJMOSFET offers the worst preconditions of the considered semiconductor designs for high frequency operation. For hard-switching applications, the high $C_{\mathrm{O(ER)}}$ results in additional losses during each transition. Still, if fast transitions could be realized, the SJMOSFET could be able to compete with the other designs since the differences are not as significant. Due to the high Q_{G} a higher gate current is required as for the other designs to achieve the same transition duration. In addition, the high C_{GD} limits the achievable transition duration for high slew rates at the drain potential. Both disadvantages could be compensated by the IFF method, making the SJMOSFET an appropriate choice as the controlled power semiconductor due to the high potential for improvement.

2.1.2 The maximum gate voltage as a limiting attribute for IFF

Accelerating the transition can be achieved by increasing i_G for both introduced control mechanisms. Thereby, the time to charge or discharge the gate is reduced, also shortening the switching duration. For the voltage controlled devices the v_{GSI} is increased faster, mostly limited by the voltage drop over the inductance of the gate connection L_G for high current gradients. This voltage drop can also limit the possible gate current due to the maximum dynamic gate-source voltage limitation $V_{GS,max,dyn}$. This value is higher than the maximum gate-source voltage limitation $V_{GS,max}$ but can only be applied for a short period. Therefore, a varying gate voltage is necessary to take advantage of the dynamic resilience. For the GaN GITs, the only current controlled design considered, the channel current during transition is directly based on the gate current, once the diode D_{GS} is conducting. For all currently available GaN GITs the maximum gate current limitation $I_{G,max}$ and the maximum dynamic gate current limitation $I_{G,max,dyn}$ are depending strongly on the R_{DSon} of the device. Again, to reduce the transition, the gate current can temporarily be increased up to $I_{G,max,dyn}$. An overview over the different limits can be seen in table 2.1:

design	SJ-MOSFET	SiC-DMOS	SiC-TMOS	GaN-HFET	GaN-GIT
V_{th} [V]	3.5	2.3	4.5	1.7	1.2
$V_{GS,max}$ [V]	-20/+20	-4/+15	0/+18	-10/+7	-10/—
$V_{GS,max,dyn}$ [V]	-30/+30	-8/+19	-5/+23	-20/+10	-25/—
$I_{G,max}$ [A]	—	—	—	—	0.02
$I_{G,max,dyn}$ [A]	—	—	—	—	2
$V_{GS,max,dyn,positive} - V_{th}$ [V]	26.5	16.7	18.5	8.3	—
$V_{th} - (V_{GS,max,dyn,negative})$ [V]	33.5	10.3	9.5	21.7	26.2

Table 2.1: Examples of dynamic and static gate limits for several current implementations.

Especially for the voltage controlled devices, it can also be useful to include the threshold voltage V_{th} to asses the suitability for the IFF method. The transistors are only conducting once v_{GSI} exceeds this threshold. The IFF method adds an additional voltage to the gate during switching by means of a transformer. The voltage delta $V_{GS,max,dyn,positive} - V_{th}$ should be the absolute maximum additional voltage added by the transformer. For most load currents the voltage has to be lower due to a higher Miller plateau voltage up to which the transformer is active during turn on. Since the devices have different transconductances, the voltage delta can not be used as an indicator for the acceleration. However, if this parameter is too small, using the IFF method can be critical. Again, the SJMOSFET offers the highest delta and therefore is especially suitable for the IFF method. If the IFF method should be also used to turn off the device, the delta $V_{th} - (V_{GS,max,dyn,negative})$ has to be taken into account as well. For the SiC devices this could be the limiting attribute, depending on the maximum considered plateau voltage.

2.2 Modeling approaches

The parasitic elements of the packaging, especially the inductance, can significantly influence the switching behavior, as stated in the beginning of the chapter. In addition, once the discrete devices are used in a circuit, the AIT adds additional parasitic elements which can influence the transition. The most critical of these elements regarding hard switching will be introduced in chapter 3.3. To take into account the impact of the AIT on the switching behavior, a correct model is necessary. This chapter will introduce and assess the modeling approaches used in this work to characterize these passive components.

In figure 2.8 the most important steps to generate a model are shown. First, the influence of the package or of the substrate have to be analyzed by either measuring the frequency response or simulate the effects by means of a electromagnetic (EM) field simulation. The frequency response characterization in this work is done with a vector network analyzer (VNA). Thereby, a higher frequency range could be measured with a better accuracy than for example with the auto balancing bridge method. An overview on different possible measurement methods can be found in [69]. A detailed description of the measurement procedure can be found in chapter 4.2.3. However, the focus of this chapter will be on a complete digital work flow. Measurements are important to verify the results, yet with simulations faster iterations and more comprehensive analyses such as Monte Carlo simulations or sensitivity analyses are possible.

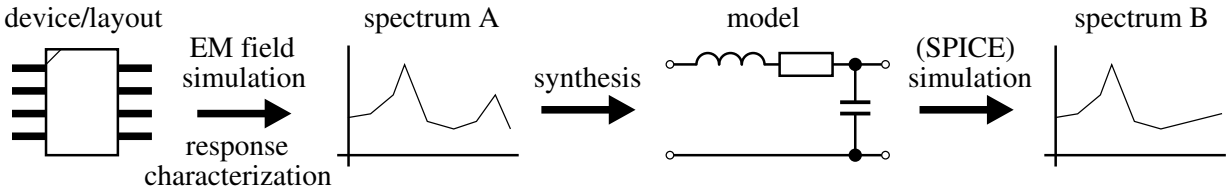


Fig. 2.8: Applied work flow to generate and validate a model of the AIT.

After a spectrum A is available for the device an equivalent circuit can be generated. Different approaches and their peculiarities are discussed in the next section. However, to achieve a simple representation based on ideal passive components, an additional synthesis can be necessary. To ensure that the models can be used in a conventional simulation program like SPICE, a lumped element model was favored wherever possible. Therefore, the accuracy of the spectrum B of a simple model decreases for higher frequencies. For the sake of simplicity and usability, this was often accepted in this work. However, a comparison with real measurements is attached, to evaluate the accuracy in the considered frequency range.

2.2.1 S-parameter generation based on electromagnetic field simulations

A 3D field simulation can be based on several algorithms. Two common concepts are the finite element method (FEM) and the method of moments (MoM). For both, a digital representation of the physical design and also ports as interfaces for external stimuli are necessary. Afterwards, each of the ports is stimulated and the resulting electromagnetic fields are computed by the algorithm. The universal S-parameters can be calculated from the amount of reflection and transmission that appears. Since S-parameter are a function of frequency, the solution can be different for every frequency step defined. The spectrum A in figure 2.8 can be extracted from the S-parameter and its accuracy depends on the amount of calculated frequency steps.

For the FEM the design as well as the surrounding material is separated into a pattern of smaller elements to create a mesh [70]. The necessary size of the mesh depends on the desired frequency range and accuracy. By using the differential form of the Maxwell equation, local solutions for every point in the mash are created and thereby the electromagnetic fields can be calculated.

In contrast to the FEM, the MoM uses the integral form of the Maxwell equations. Thereby, especially in the lower frequency domain, the design has only to be discretized at the border. A condition for the correct application of the method is a linear and homogeneous field distribution inside the material. The MoM is utilized by the Momentum simulator used in this work [71]. The simulator offers a full wave option to calculate the electromagnetic fields with all the dependencies of the Maxwell equations. The second options, which is applied throughout this work, is a quasi static calculation, using further simplifications to reduce the calculation time. A condition for the quasi static calculation is, that the electric potential does not influence the magnetic potential [72, ch. 2]. The length of the design should therefore be smaller than half the wavelength of the signal to meet this requirement ands offer accurate simulation results.

Another possible algorithm is the partial element equivalent circuit method (PEEC) [73]. An advantage of this method is that a lumped element model is already created during the analysis of the design. Therefore, no additional synthesis algorithm is necessary to create a sufficient model. However, the limitation to a lumped element model restricts the method to the lower frequency domain, similar to the quasi static approach of the Momentum simulator. This is also indicated by the different trends in the spectrum A and B of figure 2.8.

2.2.2 Synthesis of passive networks

Some conventional simulation program with integrated circuit emphasis (SPICE) tools do not support the use of S-parameter. On the other hand, different power semiconductor manufacturer optimize the simulation models for certain solver and thereby depend on appropriate SPICE tools. Therefore, a simple lumped element model can be necessary to represent the AIT and such a model furthermore reduces duration and increases convergence of the simulation.

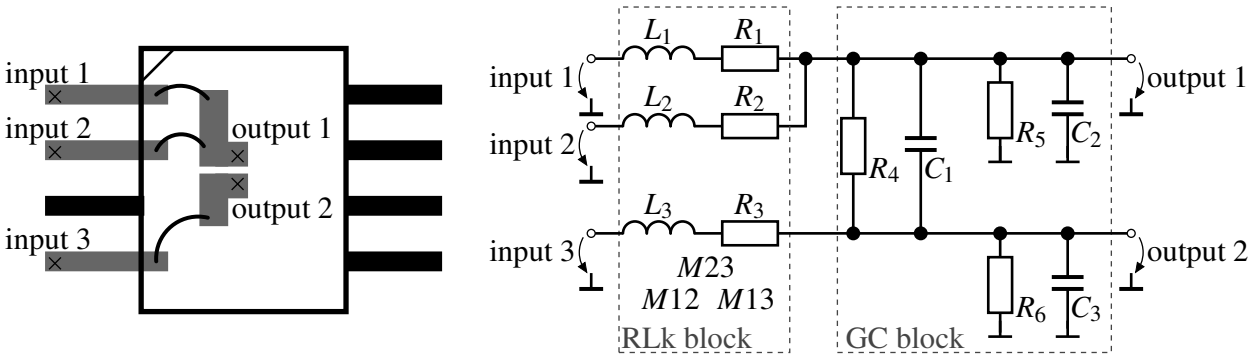
The S-parameter matrix of the design can be converted into an impedance matrix. Finding a sufficient lumped element model which accurately represents this matrix can be done by identifying the system and afterwards synthesizing a model. To identify the system, a (set of) rational function has to be determined which can be used to describe the design. This is possible for examples with the vector fitting method [74] or Prony's method [75]. Afterwards, the lumped element model is created out of these functions by a synthesis procedures. Simple lossless L-C circuits can be extracted with the technique by Foster [76]. Another approach to create ladder networks with two elements is the Cauer synthesis [77]. First models including all passive elements (R-L-C) were enabled by the Brune synthesis for two port networks [78]. Important extensions necessary for multi-port networks were developed by Tellegen [79]. Various tools which are based on this work can be found and used to extract a model from a passive network.

RLCK extraction

RLCK extraction is a tool included into the advanced design system (ADS) toolbox which is also used for the 3D field simulation [80]. With this tool, a low frequency model can be created from the S-parameter data representing the package interconnections, see figure 2.9(a). It models the structure as a RLk block followed by a GC block to ground; cf. figure 2.9(b). Mutual coupling between the different branches is considered with additional factors M. In between the RLk and GC block, the interconnections represent the fan out from inputs to outputs.

It is specified upfront whether an S-parameter port should be considered as an input or output. Package or PCB connections are usually specified as an input, semiconductor connections are typically outputs. For the resulting circuit it is assumed that the electrical reactance is constant up to first resonance frequency f_0, due to the small outlines of the layout. For electrically small antennas, numerous estimations can be found up to which size this assumption is acceptable [81]. For a frequency of 200 MHz, the wavelength λ on the PCB would be:

$$\lambda = \frac{c}{\sqrt{\varepsilon_\mathrm{r}\mu_\mathrm{r}} \cdot f_0} = \frac{299\,792\,458\,\frac{\mathrm{m}}{\mathrm{s}}}{\sqrt{5 \cdot 1} \cdot 200\,\mathrm{MHz}} = 670\,\mathrm{mm}. \tag{2.5}$$



(a) layout / AIT (b) lumped element model

Fig. 2.9: Example setup and corresponding model from RLCK extraction.

The transformer designs of this work try to comply with the limit of one quarter λ for a frequency range up to 200 MHz. With a mechanical length of around 160 mm, the maximum limit of one quarter λ is almost achieved for the secondary winding of the layout in table 4.1. Therefore, especially the inductance of this winding deviates for frequencies close to the limit. Due to the comparisons with the measurements, such deviations are highlighted. The bandwidth could also be limited to assure the lumped element model is applicable. A more conservative boundary, for example, limiting the mechanical length to one tenth of λ, could prevent deviations and ensure an accurate simulation.

3 Fundamentals of hard switching and the inductive feed-forward method

In hard-switching applications, switching losses have a significant influence on the overall losses in a power semiconductor, especially at high switching frequencies. Various concepts are known to minimize the switching duration and thereby the switching losses. Reducing the parasitic elements that influence the duration of the switching transition is a common measure. The most prominent are the gate-drain capacitance and the common source inductance, which will be introduced and analyzed later on. However, these elements cannot be eliminated completely and are often influenced by conflicting design goals, such as a reduced on-state resistance or a reduced thermal coupling. Furthermore, various modifications of the gate-driver can accelerate the transition. An active gate driver can vary the output voltage or current during the transition to realize a desired switching behavior. A controllable gate current can be realized by switchable gate resistors [31, 82] or programmable current sources [83, 84]. An adjustable gate voltage can also be a possibility if various bias voltages are available [24, 85]. However, additional logic and often a significant increase in components and protection circuitry is necessary to realize an appropriate gate driver.

The IFF method, on the contrary, manages to reduce the turn-on duration with a low component count. Only a conventional passive gate driver operating as a voltage source is necessary. An additional transformer supports the gate driver and accelerates the transition. In this chapter the basics of the IFF method will be explained as well as the important characteristics which influence the transition in hard-switching applications. To illustrate the effects of hard switching as well as the IFF method, a double pulse setup is used and simulated using SPICE. A SJMOSFET is utilized in the simulations.

3.1 Double pulse test

Double pulse measurements are a common method to determine the switching losses of power semiconductors in hard-switching applications. In the setup shown in figure 3.1, the freewheeling diode D_{FWD} forms a commutation cell with the discrete semiconductor Q. The setup can be split into a gate and a power loop that are connected by Q.

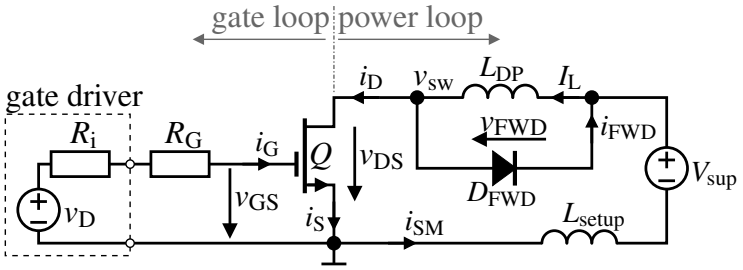


Fig. 3.1: Circuit diagram of a double pulse test setup, restricted to the essential components.

In most of the following circuit diagrams, only the gate loop is depicted. This is because changes in the gate loop, for example a different control circuit like in the IFF method, can have a significant influence on the switching losses. The power loop on the other hand is kept constant to be able to asses the influence of the changes.

The power loop is also critical for a reproducible test: In a first pulse created by the gate driver, the inductor of the double pulse test setup L_{DP} is charged to a desired load current I_{L}. Afterwards, a second pulse is utilized to characterize the switching losses at a defined current. The inductance of L_{DP} must be high enough so that the current does not significantly increase between fully turning on and off during the second pulse. Though, if the current gradient is too low and the turn-on duration is too long, self-heating of the device under test (DUT) Q can also distort the measurement. A saturation at the peak currents must also be ruled out. The use of a coreless inductor is a simple solution to this problem. By placing the coreless inductor far away from the device under test, it should also be ensured that there is no interference of the gate loop with the magnetic field formed during the double pulse test. A toroid shaped coil can help to reduce the emitted magnetic field. A capacitor parallel to the supply voltage V_{sup} may also be required to prevent a significant voltage dip during the test. Furthermore, the reverse recovery charge Q_{rr} of D_{FWD} has a significant influence on the switching losses [86] and should be kept to a minimum, especially if wide bandgap semiconductor are characterized. The fast transitions otherwise lead to a high over-current peak during turn on. However, the minimal Q_{rr} is also limited since a snap off in the diode should not occur. In such a case the switching speed would be limited because the maximum blocking voltage at the semiconductor is achieved.

A simplified representation of the most important current and voltage transitions in the double pulse test is given in figure 3.2 for a MOSFET. The first pulse is started at t_1 by slowly increasing the voltage v_{GS} controlling the semiconductor, starting at the negative bias voltage V_{Doff}. At t_2 the current i_D into the semiconductor starts to increase because V_{th} is reached, with a current gradient which is limited by the inductor L_{DP}.

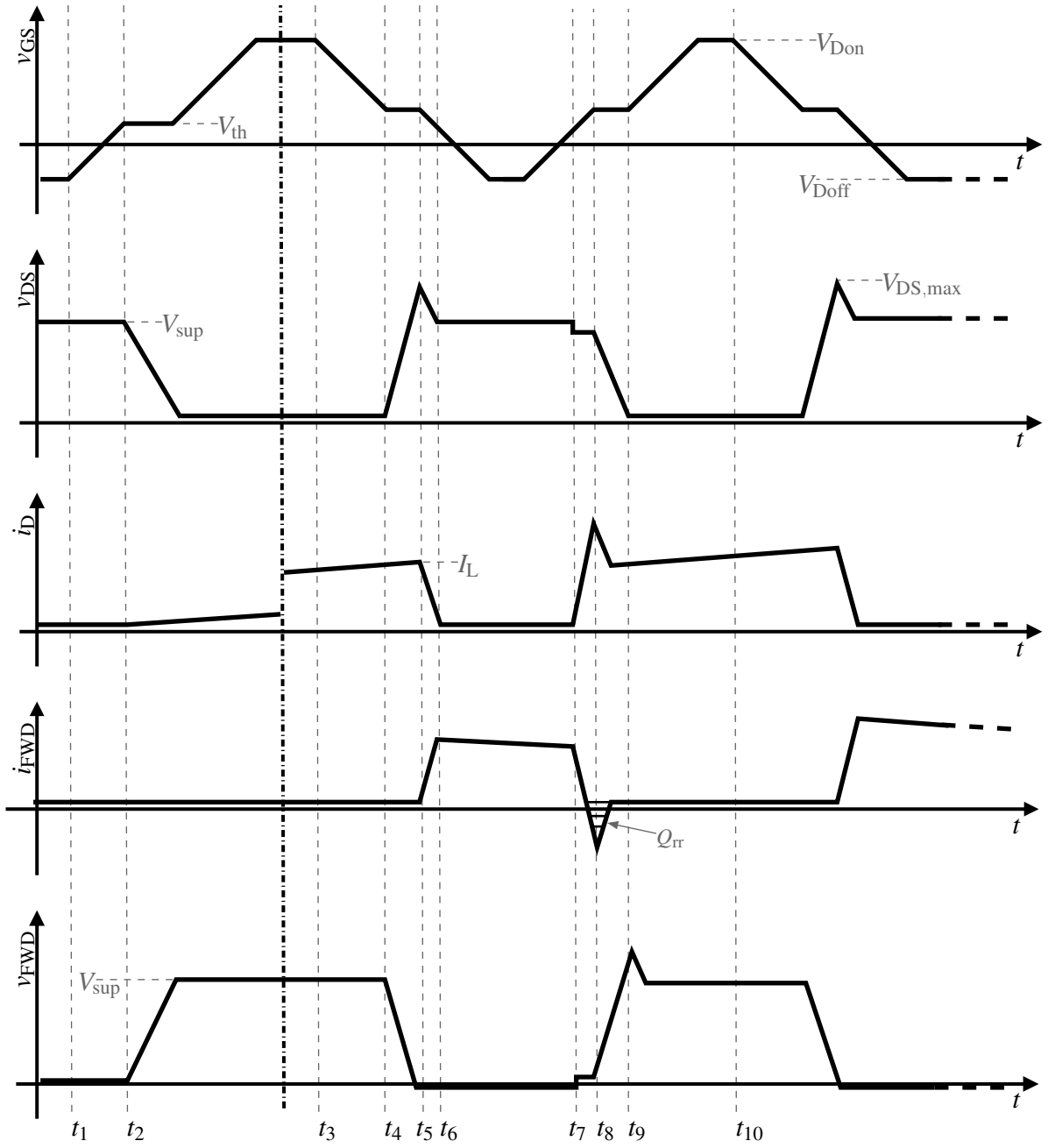


Fig. 3.2: Simplified depiction of important voltage and current transitions in a double pulse test.

To end the first pulse, the gate driver starts turning off the semiconductor at t_3 by reducing the voltage v_{GS} from the positive bias voltage V_{Don}. Once the voltage v_{GS} is low enough to switch the semiconductor from the saturation region to the ohmic region, the voltage v_{DS} increases at t_4 until the maximum drain-source voltage $V_{DS,max}$ is reached at t_5. At this time, the current i_D is turned off, beginning at I_L, which is the operating point that is used as an indicator for the switching losses. At t_6 the turn-off transition is finished. Afterwards, v_{DS} is equal to V_{sup} increased by the forward voltage of D_{FWD}, due to the current through the forward diode i_{FWD}.

To measure the turn-on characteristics, a second pulse is necessary. The turn-off duration up to the second pulse (t_6- t_7) has to be short enough to ensure that the reduction of I_L is negligible and the characteristics are measured for the same operation point. Therefore, the current drop of D_{FWD} should be minimal. The turn on starts at t_7 once v_{GS} reaches V_{th}, with an increase of the current i_D and the corresponding decrease of i_{FWD}. The current increases above I_L and reaches its peak, which is defined by Q_{rr}, at t_8. The current gradient during this period creates a voltage drop over the parasitic inductances in the commutation loop, creating a first voltage drop in v_{DS}. The final transition of v_{DS} follows the current peak and creates a voltage plateau at v_{GS} which ends at t_{10} after discharging C_{OSS} as well as further capacitances connected to the switching potential v_{SW}. Finally, the second pulse has to be terminated by turning off the semiconductor again, starting at t_{11}. Afterwards, the current in the inductor L_{DP} is slowly decreasing due to the voltage drop over D_{FWD}.

By the double pulse test, the switching losses can be determined for a defined current I_L. Often, the turn-off losses are determined between t_4 and t_6, more precisely after v_{DS} increases above a fixed value (for example 10%) up to the time that i_D dropped below a second limit. This is repeated for the turn-on losses between t_7 and t_9, only that i_D initiates the determination and v_{DS} ends it. However, this approach can be misleading and therefore in the next section more focus will be put on calculating the switching losses.

3.1.1 Switching losses

The power dissipation of the semiconductor Q in figure 3.1 is equal to the active power P_{MOS}. P_{MOS} is defined by v_{DS} and the v_{GS} as well as i_{D} and the i_{G}:

$$P_{\mathrm{MOS}}(t) = i_{\mathrm{D}}(t) \cdot v_{\mathrm{DS}}(t) + i_{\mathrm{G}}(t) \cdot v_{\mathrm{GS}}(t). \tag{3.1}$$

The gate current can often be measured using the external gate resistance R_{G}. Measuring i_{D} is more complicated, especially if devices should be characterized at higher blocking voltages. To avoid significant isolation, the source current i_{S} can be used to substitute i_{D}:

$$i_{\mathrm{S}}(t) = i_{\mathrm{D}}(t) + i_{\mathrm{G}}(t) \quad \Rightarrow \quad P_{\mathrm{MOS}}(t) = i_{\mathrm{S}}(t) \cdot v_{\mathrm{DS}}(t) - i_{\mathrm{G}}(t) \cdot v_{\mathrm{DS}}(t) + i_{\mathrm{G}}(t) \cdot v_{\mathrm{GS}}(t). \tag{3.2}$$

If it can be ensured that the gate driver is isolated sufficiently and therefore only minimal leakage current occurs, another approach can be that the measured source current i_{SM} is used to replace i_{D}:

$$P_{\mathrm{MOS}}(t) = i_{\mathrm{SM}}(t) \cdot v_{\mathrm{DS}}(t) + i_{\mathrm{G}}(t) \cdot v_{\mathrm{GS}}(t). \tag{3.3}$$

The switching losses can now be determined during the transition period:

$$E_{\text{turn-off}} = \int_{t_0 - t_n}^{t_0 + t_p} P_{\mathrm{MOS}}(t)\, dt. \tag{3.4}$$

The integration limits t_{n} and t_{p} refer to the point in time t_0 when v_{DS} is equal to half of V_{sup}. The turn-off energy $E_{\text{turn-off}}$ is determined during a rising voltage slope of v_{DS}. The turn-on energy $E_{\text{turn-on}}$ can be determined accordingly during a falling voltage slope with adjusted integration limits. It has to be ensured that the transition is completed during the integration period. Fixed integration limits provide a good comparability for varying transition duration of Q.

An example of a hard-switching transition in a double pulse sequence is shown in figure 3.3. In this example, the turn-off losses are determined after the turn-on losses different to the example in figure 3.2. The negative integration time t_{n} and the positive integration time t_{p} for the turn-off transition are marked. $E_{\text{turn-off}}$ is determined from equation 3.1 and for $E_{\text{turn-on}}$ shorter integration limits are chosen, due to a faster transition. Furthermore, the share of $i_{\mathrm{G}}(t) \cdot v_{\mathrm{GS}}(t)$ is often neglected in this work because it is marginal.

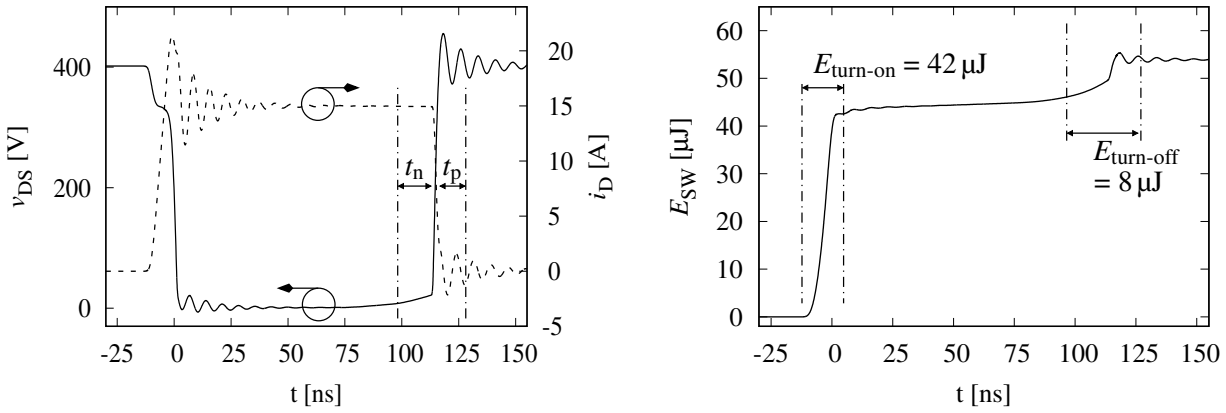
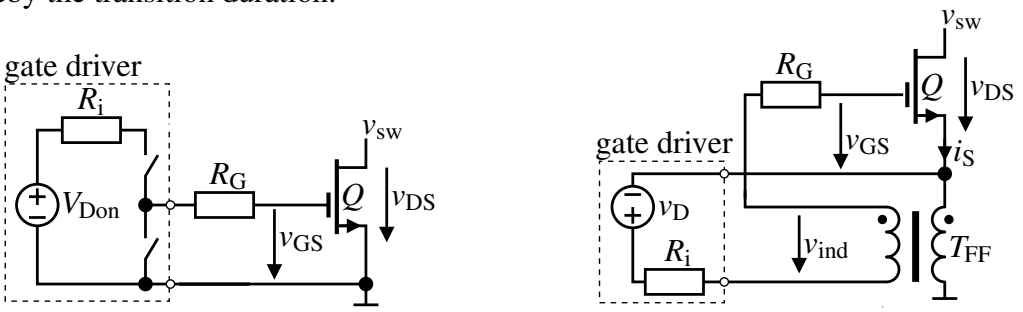


Fig. 3.3: Example of the switching transitions and corresponding losses for I_L= 15 A.

Often instead of fixed integration limits, voltage and current limits are used to determine the switching losses. For example, $E_{turn\text{-}off}$ has to be determined after V_{sup} increases above 10 % of V_{sup} until i_D drops below 10 % of I_L [87]. However, especially for the selected SJMOSFET, the turn-off losses already increase significantly before the drain-source voltage reaches 10 % of V_{sup}. Therefore, fixed integration limits are favored in this work to ensure a correct and reproducible determination of the losses. Furthermore, a correct deskew of the measurement probes is essential, to prevent an incorrect interpretation of the measurement data. To achieve this, a defined current pulse can be measured over a shunt close to the current probe with a voltage probe to align both.

3.1.2 Simulation schematic

In this section the simulation schematic used in this work for the double pulse setup will be introduced. A simple realization of a conventional gate driver is shown in figure 3.4(a). The voltage source V_{Don} in combination with a controlled half bridge creates a voltage pulse with the desired duty cycle and frequency. An additional resistor R_G limits the gate current of the semiconductor Q and thereby the transition duration.



(a) conventional (b) inductive feed forward

Fig. 3.4: Comparison of the gate driving methods used in this work.

The IFF method uses only an additional feed-forward transformer T_{FF} to accelerate the turn-on transition. The transformer is introduced between the source and gate of Q; see figure 3.4(b). During the switching transition, the gradient of i_S in the primary winding results in an induced voltage v_{ind} in the secondary winding. The polarity of the transformer T_{FF} is chosen so that it adds a positive voltage to the gate during turn on and a negative voltage during turn off. The gate driver in this figure is identical to the conventional approach but was simplified to a voltage source providing a pulsed gate driver voltage v_D.

A simplified representation of the double pulse simulation schematic is presented in figure 3.5. The additional impedance of the PCB, was computed through the Momentum 3D planar electromagnetic simulator.

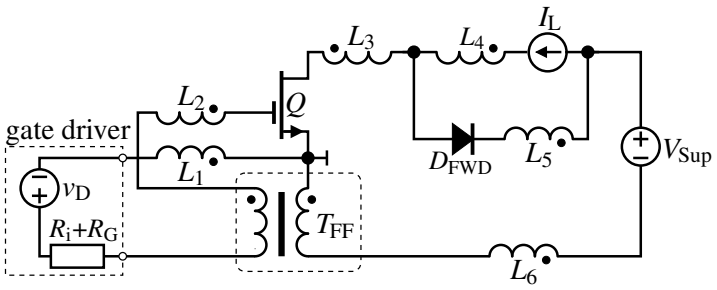


Fig. 3.5: Schematic of the simulation for the double pulse test setup, restricted to the essentials.

The simulation schematic corresponds to the circuit diagram in figure 3.1. The inductor of the double pulse test setup L_{DP} is replaced by a current source, providing the desired I_L. The gate driver is replaced by a simple pulsed voltage source switching from 0 V to V_{Don} and back. The optional transformer T_{FF} can be added to realize the IFF method. A detailed model of T_{FF} will be introduced in chapter 4.2.4. The primary winding is added to the power loop and the secondary winding to the gate loop. Furthermore, the circuit is extended by the inductors L_1-L_6, representing the inductance added by the PCB. Thereby a more detailed representation of the parasitic inductance of the setup L_{setup} is possible as also proposed in [88]. The corresponding parameters are given in table 3.1. If significant, the coupling coefficient k is also added and its subscript corresponds to the involved inductors. Therefore, k_{12} is the coupling coefficient between L_1 and L_2. Additional capacitors representing the capacitance added by the PCB to the switching potential as well as to the gate can also be necessary. However, for the chosen layout these have been insignificant and therefore could be neglected.

L_1	L_2	L_3	L_4	L_5	L_6	k_{12}	k_{34}	k_{36}	k_{46}
6.6 nH	5 nH	5 nH	2.7 nH	2.5 nH	4.9 nH	0.36	0.78	0.29	0.29

Table 3.1: Inductance and coupling coefficients of the double pulse simulation.

For every inductor a resistor was added in series. To keep the schematic clean, these are not shown. The parameters are given in table 3.2.

R_G	R_{L1}	R_{L2}	R_{L3}	R_{L4}	R_{L5}	R_{L6}
10 Ω	18 mΩ	61 mΩ	10 mΩ	6.5 mΩ	6 mΩ	80 mΩ

Table 3.2: Resistance values of the double pulse simulation.

To finalize the simulation schematic, the simulation model of the discrete semiconductor Q has to be included. If the model does not contain the package inductances of the device, these have to be added separately as shown in figure 2.1. For the ThinPak 8x8 package this results in the following values [89, 90]:

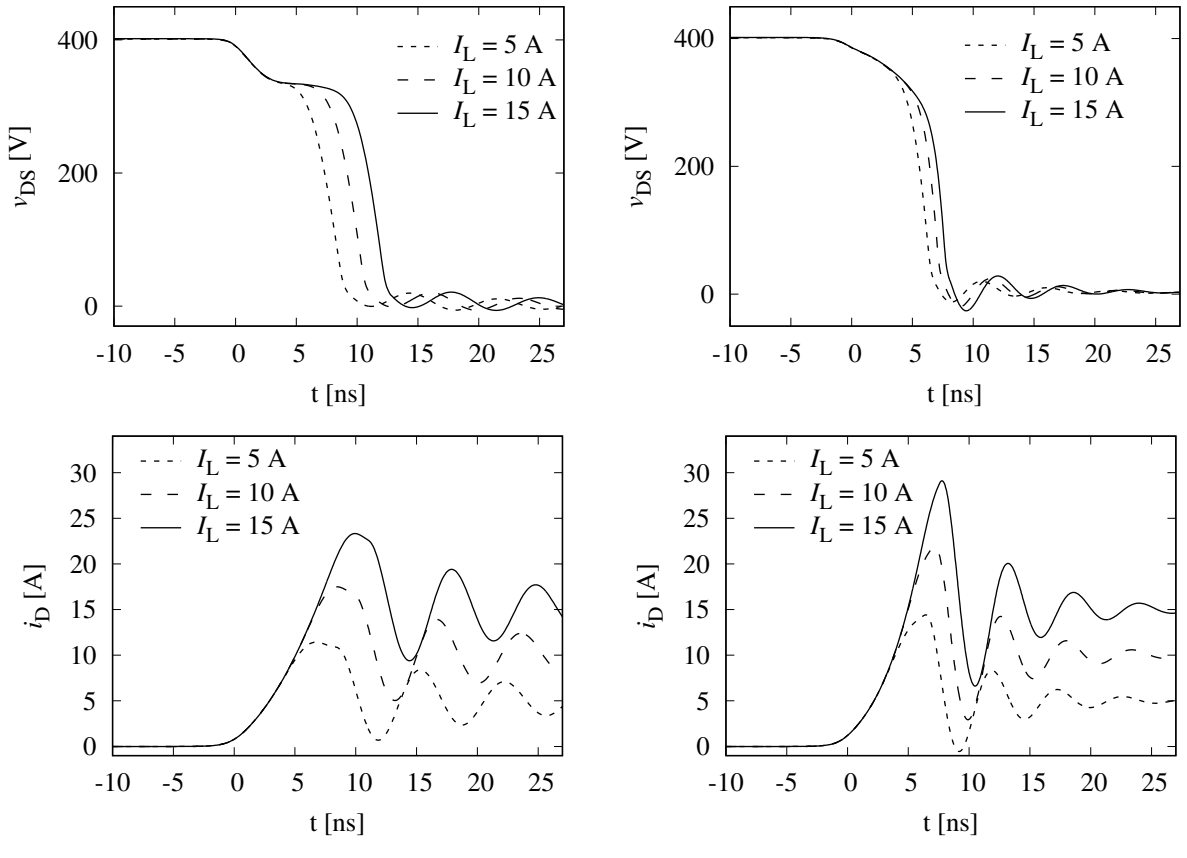
L_D	L_{CS}	L_K	L_G
500 pH	2 nH	5 nH	5 nH

Table 3.3: Additional inductances for discrete semiconductors in a ThinPak 8x8 package.

If the semiconductor is susceptible to ringing, an additional 1 Ω resistor in parallel to the inductors L_1-L_6 can be used to emulate the skin effect and dampen oscillations. This value was chosen based on the results in chapter 4.2.4. This can be necessary since, the circuit can only be characterized as lumped elements up to 10 MHz; cf. chapter 2.2.2. A more detailed analisis of this approach will be given later on in chapter 4.2.4.

3.2 Influence of the IFF method on the switching transition

The double pulse setup in figure 3.1 can be easily extended by T_{FF} to realize the IFF method as shown in figure 3.4. A direct comparison with the conventional approach is given in this chapter by comparing the simulation results. To show the different switching characteristics of both gate driving setups during hard switching, the voltage and current transitions are displayed in figure 3.6. First, the turn-on transition is analyzed since the IFF method has a major impact. For the conventional approach in figure 3.8(a), the current i_D increases until a constant gradient is achieved. This gradient is the same for all the illustrated I_L. The steady gradient results in a constant voltage across the inductance L_{setup}; see figure 3.1. This voltage is equal to the first voltage drop of v_{DS} since the forward voltage of the diode D_{FWD} is marginal in this voltage range. After i_D exceeds I_L, v_{SW} is discharged, resulting in the second voltage drop.

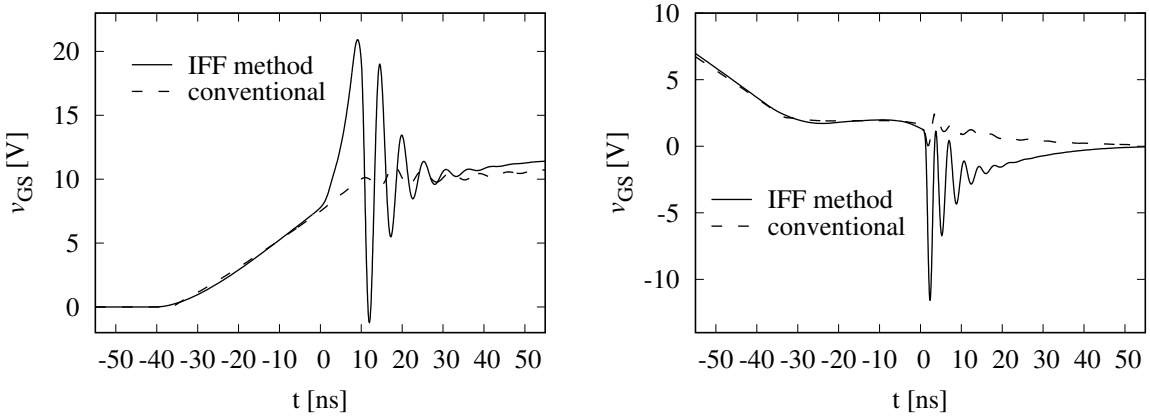


(a) conventional (b) inductive feed forward

Fig. 3.6: Comparison of v_{DS} and i_D for both gate-driving methods during the turn-on transition.

In contrast to the constant current gradient of the conventional approach, the chosen transformer T_{FF} results in a gradually increasing gradient of i_D in figure 3.8(b). Therefore, instead of showing an intermediate voltage plateau, the IFF method results in a single voltage drop of v_{DS}. For increasing I_L the transition duration is reduced with the IFF method, even though the current peak of i_D is also significantly increased.

The explanation for the faster turn-on transition can be found by looking at the gate voltages in figure 3.7(a). Once the current i_D rises at around 0 ns, this results in a strong rise of v_{GS} for the IFF method, accelerating the transition. The conventional approach, on the other hand, shows only a steady increases in the gate voltage until it reaches the Miller plateau level.



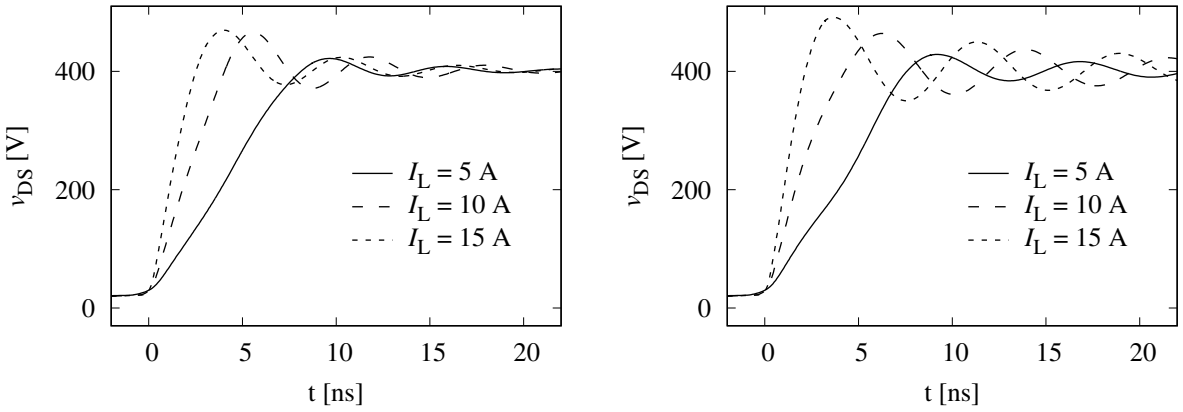
(a) turn on (b) turn off

Fig. 3.7: Influence of the IFF method on the gate voltage v_{GS} for I_L = 15 A.

During the Miller plateau phase, starting at around 10 ns, the gate driver is only discharging C_{GD}, without charging the gate-source capacitance C_{GS}. This results in a constant v_{GS} and the operation point controls the slew rate of the device for the conventional approach. The IFF method also displays a comparable Miller plateau phase following the induced voltage peak, even though additional ringing is superimposed on the actual voltage of the plateau. The higher slew rate indicates a higher v_{GSI} and the transition is further accelerated due to a shorter plateau phase.

Furthermore, in figure 3.7(b) the influence of the turn-off transition on the gate voltage is shown. The corresponding switching characteristics can be seen in figure 3.8. As intended, the transformer of the IFF method adds a negative voltage during the current transition. Contrary to the turn-on transition, the impact of the IFF method on the turn-off losses is minimal. The voltage transition is mainly defined by the load current I_L. Once the i_{CH} of the power semiconductor is reduced, C_{OSS} is charged immediately. Thereby, the transition duration can be significantly shorter compared to turn on. Yet the influence of the additional transformer should not be disregarded. T_{FF} adds to

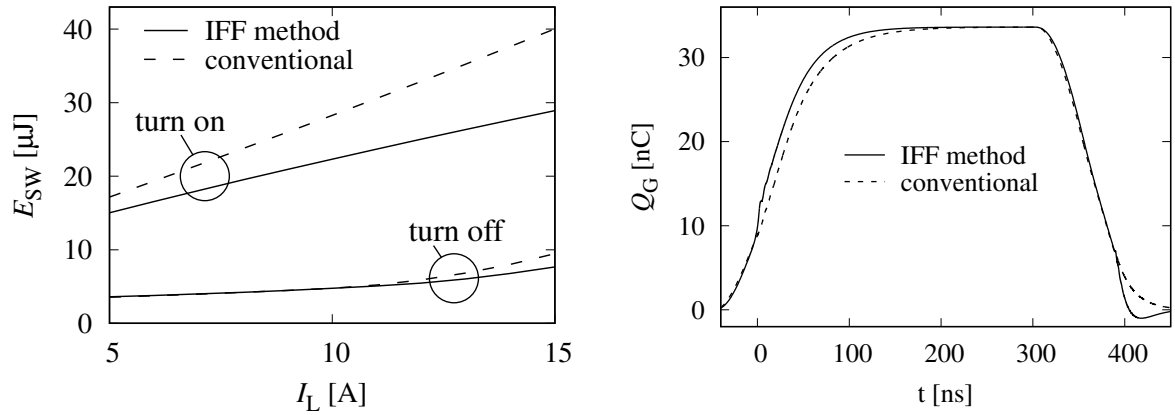
the inductance L_{setup} which is accountable for the overvoltage peak, and the additional inductance should therefore be in proportion to the other shares of L_{setup}.



(a) conventional (b) inductive feed forward

Fig. 3.8: Comparison of v_{DS} for both gate-driving methods during the turn-off transition.

Even for the maximum considered load current, the final slew rate of the turn-off transition is much lower than that during the turn-on transition and not as dependent on the gate voltage. This is also reflected in the switching losses that can be found in figure 3.9(a). The reduction of the turn-on losses is clearly noticeable and more significant. That the turn-on losses are more substantial than the switching losses is also true for the other considered unipolar semiconductor designs [21].



(a) switching losses (b) I_{L}= 15 A

Fig. 3.9: Composition of the switching losses and course of the gate charge during switching.

The influence of the IFF method on turn off is strongest close to the maximum load current. On the other side, the turn on benefits already for low load currents from the accelerating effect of the IFF method. $Q_{\text{G}} = \int i_{\text{G}}(t)\, dt$ is also shown in figure 3.9(b). Comparing both methods in terms of the progression of Q_{G} illustrates once again the accelerating effect of the IFF method. Furthermore, the

ringing which affects especially the gate voltage is filtered and therefore the accelerating influence on the gate can be identified.

For the turn-off transition, the SJMOSFET is not the most suitable choice of the considered power semiconductor designs. There are designs with a lower $C_{O(ER)}$ which could result in an increasing impact on the turn-off transition (cf. chapter 2.1.1). The discharging of C_{OSS} would be accelerated, leading to an earlier current gradient and thereby faster impact of the IFF method. However, the transition is slowed down by the slew rate. The slew rate during turn off is dependent on C_{OSS} and rises according to the load current. For higher load currents, a power semiconductor with a reduced R_{DSon} is chosen. Because of the simultaneously higher C_{OSS} and therefore lower slew rate during turn off, the influence of the IFF method on turn off would be reduced again.

3.3 Important characteristics affecting hard switching

To understand how the IFF method decreases the switching duration, the model elements which affect the transition during hard switching have to be known and their impact classified. Therefore, this chapter expands on the important parasitic elements as well as some common strategies to optimize a setup for hard switching. Again, the simulation setup from figure 3.1 is adapted for the different analyses. The model elements are already introduced in chapter 2; cf. figure 2.1. Since a SJMOSFET is used for the analysis, the impact of the parasitic elements can be different for the other considered designs. However, the trends should be comparable for all semiconductor controlled by the field effect. Furthermore, the (over-)compensating effect of the IFF method on the impact of the parasitic elements is estimated, mostly based on the progression of Q_G and the switching losses. To give an overview regarding the effect of the elements on the switching characteristics, the graphs of figure 3.9 provide most of the substantial information, and are therefore used as a reference.

3.3.1 Drain-source capacitance

The drain-source capacitance (C_{DS}) has no direct influence on the gate charge. Still, the effect on the switching losses is significant since it effects the transition. First, the voltage transition is correlated to drain-source capacitance C_{DS}, since it is normally the more significant part of C_{OSS}; cf. chapter 2.1.1. A high capacitance results in a lower slew rate for the same load current and therefore slower transitions. By affecting the slew rate, C_{DS} also influences the gate charge by shaping the current in C_{GD}. Secondly, C_{OSS} affects the transition due to the overall charge. During switching the capacitance needs to be (dis)charged and therefore prolongs the current transition. Thereby, the duration during which L_{CS} effects the transition is extended. Since the IFF method accelerates the transition, both effects can be compensated and the method is therefore especially suitable for devices with high C_{DS}. An exception is the turn off, since in hard-switching applications, for light load currents the slew rate is defined by C_{DS}. This is because even when the semiconductor is already turned off, C_{DS} still needs to be charged. In this special condition, a low C_{DS} also lowers the load current above which the IFF method can effect the transition; cf. figure 3.9.

3.3.2 Gate-drain capacitance

The second important characteristic is the gate-drain capacitance C_{GD}, which mostly depends on the semiconductor design as well as the on resistance; cf. figure 2.7. The AIT can also add to the characteristic, but the influence is normally insignificant. The influence of an increased capacitance is simulated by an additional parallel capacitance C_{GD2}, see figure 3.10.

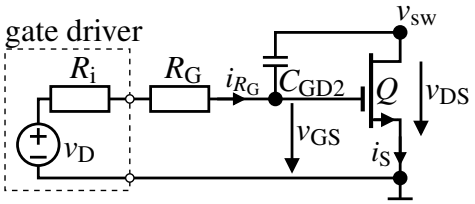


Fig. 3.10: Gate loop with additional gate-drain capacitance.

Due to the total gate-drain capacitance, voltage transitions introduce a current to the gate of the semiconductor. Thereby, the so called Miller plateau is created. This is a constant voltage level of v_{GS} which is created because the current from the gate driver i_{RG} is necessary to charge C_{GD} instead of C_{GS}; cf. figure 3.7. The impact which an increased C_{GD} has on the gate charge and the switching losses can be seen in figure 3.11. Due to the higher capacitance, the necessary charge to turn on the device increases. Furthermore, the transition is slowed down resulting in higher switching losses. Due to the low impedance of the gate loop in this simulation, the additional charge is supplied almost instantly by the gate driver, resulting in a steep increase of the gate charge for C_{GD2} = 20 pF. If the impedance is higher, this increase of Q_G is slower, resulting in an even steeper trend of the switching losses.

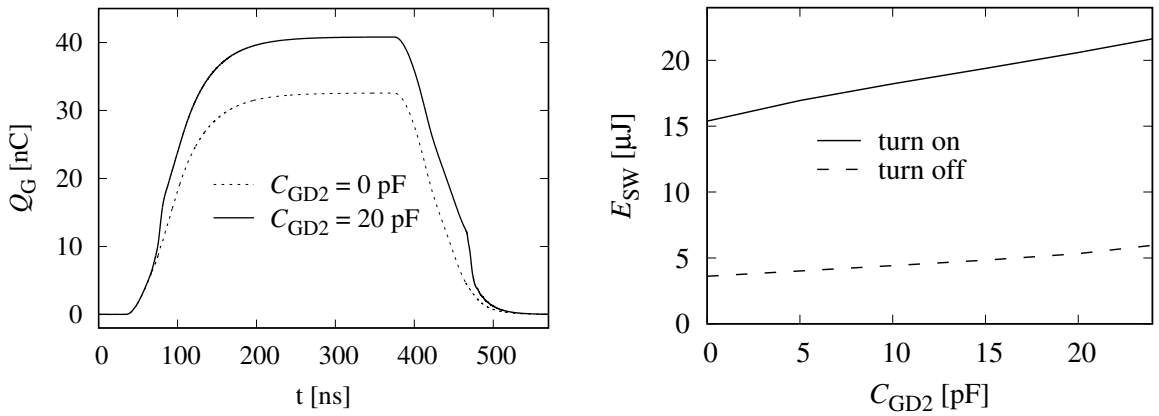


Fig. 3.11: Influence of C_{GD} on the switching characteristics, with I_L = 5 A while simulating Q_G.

The current through C_{GD} increases for faster voltage transitions and prolongs or even interrupts the switching. A higher gate current can minimize this effect. This can be achieved by reducing the impedance of the gate loop or increase the (negative) voltage of the gate driver. The IFF method is another option and accelerates the charging of the gate. Thereby high C_{GD} are compensated making the method particularly effective for these types of power semiconductors.

3.3.3 Common source inductance

An important parasitic element slowing down switching is the common source inductance L_{CS}. In addition to the discrete package, the circuit can add to the L_{CS}, increasing the impact. In figure 3.12 a conventional voltage gate driver setup is shown, for which L_{CS} has a significant influence on the transition duration.

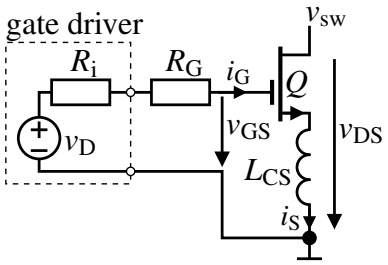


Fig. 3.12: Gate loop with additional common source inductance.

The gate driver controls v_{GS} and i_G is limited by R_G. During switching the current gradient of i_S creates a voltage drop over L_{CS}. Thereby, v_{GSI} (cf. figure 2.1) is affected which can also be seen by observing Q_G in figure 3.13.

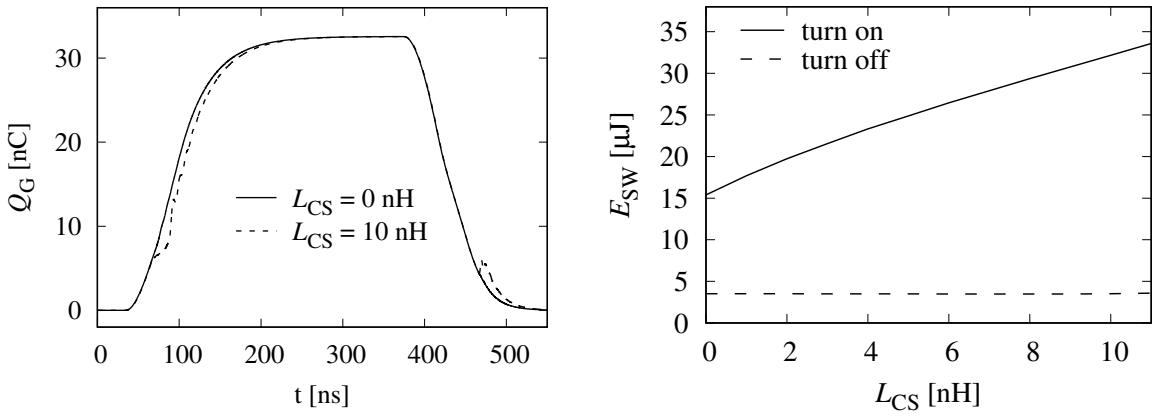


Fig. 3.13: Influence of L_{CS} on the switching characteristics, with $I_L = 5$ A while simulating Q_G.

Without L_{CS}, the gate is charged almost constantly from 0 V to 12 V during the turn-on transition and afterwards discharged during turn off. After increasing L_{CS} up to 10 nH, during turn on the

charging of the gate is slowed down once the Miller plateau is attained, which is clearly visible at around 6 nC. Due to the increasing i_S, there is a voltage drop over L_{CS} reducing v_{GSI} and thereby the charging of Q_G. During turn off an additional charge is added to the gate due to L_{CS}. However, the impact on the switching losses are different for both transitions. With increasing L_{CS} the turn-on losses are steadily increasing. The turn-off losses on the other hand are not influenced. This is because during turn off the drain current keeps constant for a while to charge C_{OSS}. Since I_L is low, the transition duration is defined by the charging duration and the impact of L_{CS} is negligible. The current gradient arises after the gate is already further discharged and therefore the transition is not delayed. This can change for higher load currents and also depends on the C_{OSS} of the device. As already stated, a Kelvin contact and/or a leadless packages are commercially available solutions to reduce or remove the effect of L_{CS}.

3.3.4 Commutation loop

While introducing the double pulse setup, the circuit was split into a gate loop and a power loop, see figure 3.1. An important characteristic of the power loop is the inductance of the commutation loop L_{setup} which is a composition of several inductances. In the simulation setup of figure 3.5 the inductors L_3-L_6 represent the proportion of the PCB layout. Furthermore, the inductances L_D and L_{CS}, cf. figure 2.1, represent the proportion of the discrete semiconductor, which needs to be added for Q and D_{FWD} separately. A design goal for hard-switching applications is to keep L_{setup} minimal. This is because it influences the over-voltage peak during turn off, as already mentioned earlier. Furthermore, it affects the ringing of the current due to the resonant circuit which is created by Q, D_{FWD} and L_{setup}. Following [91], the resonance frequency can be estimated with:

$$f_{com} \approx \frac{1}{2\pi\sqrt{L_{setup} \cdot C_{OSS}}}. \tag{3.5}$$

Overall, the inductance of the commutation loop should be kept minimal to achieve a high resonance frequency. The higher frequency domain is not stimulated as much during hard switching, a trend can be seen in figure 6.15. Furthermore, the dampening is normally also increased for higher frequencies due to the skin effect. Therefore, for PCB layouts there are numerous publications how to optimize the commutation loop. For example, the PCB can follow either a lateral or vertical design [92] or even a multi-layer approach [93]. Overall, a high width and low distance are beneficial for the conductor contributing to the loop [94]. Since the primary winding of the transformer T_{FF} directly adds to L_{setup}, its inductance has to be kept minimal. Thereby, the over-voltage peak can be limited and the current ringing is dampened due to a higher f_{com}.

3.3.5 The importance of the gate loop inductance for oscillation

Similar to the commutation loop, the gate loop also forms a resonant circuit. This time the main contribution to the inductance is by the inductors L_1 and L_2 of figure 3.5. The coupling factor k_{12} between both indcutors will be neglected in this section. Again, the proportions added through L_K and L_G of Q have to be considered and the gate driver can also add significant inductance. If the gate driver can be considered as an ideal voltage source, only C_{GS} has to be considered for the effective capacitance. Otherwise, the buffer capacitance for the positive gate driver supply C_{on} has to be taken into account for turn on and the buffer capacitance for the negative gate driver supply C_{off} for turn off. In figure 3.14 an overview of the different proportions adding to the resonant circuit is shown for the conventional approach.

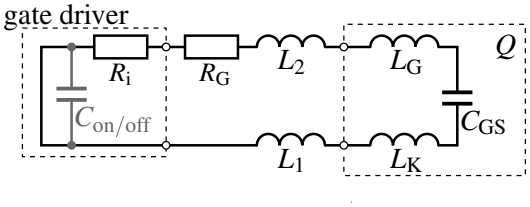


Fig. 3.14: Equivalent circuit of the gate loop for the conventional approach.

Again, the resonance frequency of the gate loop results from the sum of the involved reactances:

$$f_{gate} \approx \frac{1}{2\pi\sqrt{(L_1+L_2+L_K+L_G)\cdot C_{GS}}}. \tag{3.6}$$

Furthermore, the damping factor D can be obtained by taking the participating resistances into account [95]:

$$D = \frac{R_i+R_G}{2}\cdot\sqrt{\frac{C_{GS}}{(L_1+L_2+L_K+L_G)}}. \tag{3.7}$$

For D = 1 the gate loop is critically damped and the gate is protected from a v_{GS} overshoot. However, to compensate C_{GD} and especially the miller current during turn on, a low impedance can be beneficial and a lower damping can be advantageous. Overall, the gate loop inductance should be kept minimal to increase the resonance frequency and thereby utilizing the skin effect which supports the damping.

A disadvantage of the IFF method is that it adds additional inductance to the gate loop and even the capacitance can be increased significantly if not considered in the design of T_{FF}. Since the

coupling capacitance between primary and secondary winding of T_{FF} is parallel to C_{GS} it increases the effective capacitance and further reduces the resonance frequency of the gate loop. Due to these reasons it is critical to optimize the design of T_{FF} to achieve a high resonance frequency and thereby also improved damping due to the skin effect. Especially for power semiconductors with an already high C_{GS} which are therefore susceptible for oscillations at the gate.

4 Coreless planar transformer

Printed spiral winding inductors are a good starting point when looking into transformers designs for PCB. These inductors are used to construct transformers for switched mode power supplies operating at high switching frequencies. The designs try to achieve an inductance of the primary and secondary windings in the range of several hundred nanohenry or even microhenry (cf. [96–98]) either with [99] or without [98] a magnetic core. For these transformers, interwinding capacitance has already been recognized as a significant parameter limiting the bandwith. Alternating the windings can be a solution to reduce this capacitance and thereby increase the bandwith [100]. Another important element of the transformer is the coupling capacitance. It is a current path for common mode noise and can thereby disturb surrounding circuitry [101]. Furthermore, this work will show that the coupling capacitance is also influencing the bandwidth of the transformer. Due to the high primary inductance, spiral winding inductors are not particularly advantageous for the IFF method since the inductance of the commutation loop and thereby the overvoltage peak during turn off would be increased significantly.

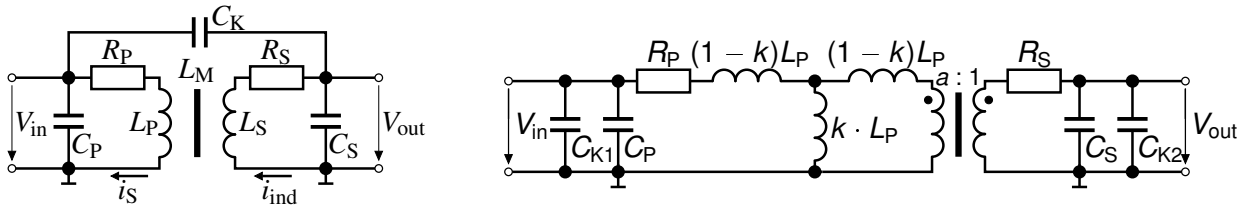
Lately, coreless planar transformers are also used in current sensors for power semiconductors. A main characteristic of the designs is how much inductance they add to the commutation loop. A four-layer design encapsulating the secondary winding inside the primary winding is presented in [102]. However, especially the necessity of buried vias increases the cost significantly. Furthermore, in [102], the pickup coil is placed next to the main conductor. This design can be expanded to a figure-of-eight shape with turns on both sides of the conductor [103]. A disadvantage of both versions is that adjacent current-carrying conductors also strongly couple into the pickup coil. In [104] the secondary winding is placed underneath a lateral power loop, realizing a two-layer design. Nevertheless, for vertical commutation loops, a four-layer PCB is still necessary.

It has been shown that coreless planar transformer realized on a PCB is suitable for the IFF method [25]. FR-4 as a substrate offers a flat and reproducible design due to tight tolerances during the manufacturing process [105]. Only the frequency dependency of the PCB strongly depends on the material used by the manufacturer [106]. In this chapter a novel coreless planar transformer will be

presented which offers inexpensive production and easy implementation for vertical commutation loops. Therefore, the layout of the design was restricted to two layers. Furthermore, the design increases the bandwidth by reducing the coupling capacitance.

4.1 Lumped element model

In figure 4.1(a), the applied lumped element model which will be used to further analyze the coreless planar transformer can be seen. The two transformer windings are characterized by the inductance of the primary winding L_P and the inductance of the secondary winding L_S. L_P and L_S are coupled by the mutual inductance L_M. The winding resistance is modeled by R_P for the primary winding and R_S for the secondary winding. As no magnetic core is used, the core loss resistance in the traditional low-frequency model is ignored. For high-frequency operation the interwinding capacitances C_P and C_S for the primary and secondary windings have to be included. Additionally, the coupling capacitance C_K between the two windings can have a significant influence.



(a) lumped element model (b) equivalent circuit

Fig. 4.1: Model and equivalent circuit of the coreless planar transformer.

To describe the influence of the different designs on the transfer characteristics, the equivalent circuit in figure 4.1(b) is used. For the mutually coupled inductors, a T circuit using an ideal transformer with the turns ratio $a = \sqrt{L_P/L_S}$ was chosen. Since $L_M = k\sqrt{L_P \cdot L_S}$ where k is the coupling coefficient, the magnetizing reactance can be described as $a \cdot L_M = k \cdot L_P$. Also, the series loop impedances can be simplified to $(1-k) \cdot L_P$. Thus, the benefit of increasing the coupling coefficient to amplify the amplitude of the output voltage V_{out} for a given L_P becomes obvious. The coupling capacitance C_K was split into C_{K1} and C_{K2} through Miller's theorem:

$$\frac{1}{C_{K1}} = \frac{1}{C_K} \cdot \frac{1}{1-f_T} \quad \text{and} \quad \frac{1}{C_{K2}} = \frac{1}{C_K} \cdot \frac{f_T}{f_T - 1} \quad \text{where} \quad f_T = \frac{V_{out}}{V_{in}}. \tag{4.1}$$

The transfer function f_T can be found in [96]. In addition, the source current i_S and induced current i_{ind} in figure 4.1(a) can be used to describe the voltages V_{in} and V_{out}:

$$V_{in} = L_P \cdot \frac{di_S}{dt} - L_M \cdot \frac{di_{ind}}{dt} + i_S \cdot R_P \quad \text{and} \quad V_{out} = L_M \cdot \frac{di_S}{dt} - L_S \cdot \frac{di_{ind}}{dt} + i_{ind} \cdot R_S. \tag{4.2}$$

If i_{ind} is kept minimal and R_P can also be neglected, equation 4.1 and equation 4.2 can be simplified:

$$V_{in} \approx L_P \cdot \frac{di_S}{dt} \quad \text{and} \quad V_{out} \approx L_M \cdot \frac{di_S}{dt} \quad \Rightarrow \quad f_T = \frac{L_M}{L_P}. \tag{4.3}$$

Therefore, the coupling capacitance can be split into:

$$C_{K1} = C_K \cdot \frac{L_M - L_P}{L_P} \quad \text{and} \quad C_{K2} = C_K \cdot \frac{L_M - L_P}{L_M}. \tag{4.4}$$

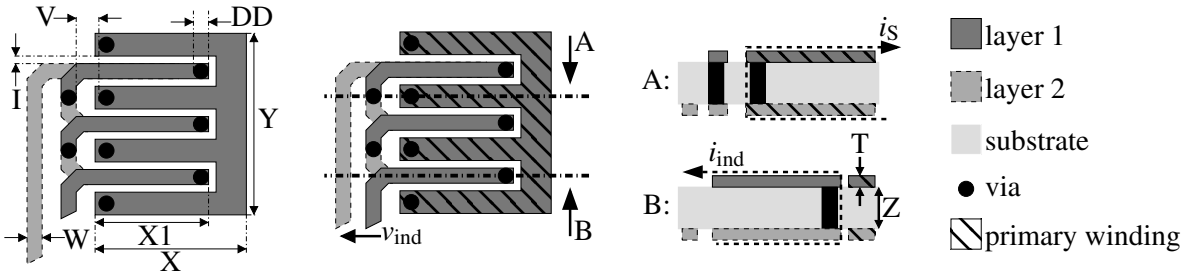
An important characteristic is the f_0, which for most applications limits the maximum bandwidth. Since C_{K2} is in parallel to the output capacitance, its influence on f_0 cannot be neglected. Therefore, according to [107] f_0 can be found at:

$$2\pi f_0 = \sqrt{\frac{1}{L_0 C_0}} \quad \text{where} \quad L_0 = L_S \quad \text{and} \quad C_0 = C_{K2} + C_S. \tag{4.5}$$

The current i_{ind} increases significantly at the first resonance frequency. Therefore, the simplification of equation 4.3 is not applicable anymore. Still, it can be helpful to understand the dependencies of C_{K1} and C_{K2} as well as to get an estimation for f_0.

4.2 Novel design of a coreless planar transformer

The novel design of a coreless planar transformer that only requires a two-layer substrate is shown in figure 4.2. The distances and edge lengths necessary to describe the dimensions are depicted in figure 4.2(a). To understand the design principles, the simple layout of the structure in figure 4.2(b) with the cross sections A and B is sufficient. The primary and secondary windings of the transformer are placed next to each other in opposite directions. The layout of the primary winding is identical for the top and bottom layers (layers 1 and 2) and is highlighted by hatching. To increase the inductance of the primary winding, the design of the secondary winding (without hatching) could also be applied to the primary winding. The figure displays a single primary winding interleaved with the turns of the secondary winding. The input and output of i_S are on one side of the substrate as seen in cross section A of figure 4.2(c). The induced current (i_{ind}) through the secondary winding can be seen in cross section B.



(a) dimensions (b) top view (c) cross sections

Fig. 4.2: Layout of the novel coreless planar transformer.

The biggest advantage of the new design over previous coreless planar transformers is the restriction to two layers. Thereby, inexpensive production and easy implementation is possible for a lot of substrates, especially FR-4. However, some constraints are necessary to keep the costs down. Most PCB manufacturer increase the price if small drill diameters are requested. Since drilling the holes is a serial process, small diameters can increase the drill count and thereby the machine time. Therefore, the drill diameter (DD) was set to 0.25 mm; compare figure 4.2(a). An additional annular ring is necessary. Furthermore, the minimal distance (e. g. I) and diameter (e. g. W) of layout structures is often limited by the manufacture depending on the copper thickness (T). The thickness of the substrate (Z) is sometimes also an important factor in pricing. Considering these restrictions, the dimensions of a low cost transformer design are given in table 4.1.

X	X1	Y	Z	DD	N	W	I	V	T
11.5 mm	10 mm	10 mm	1 mm	0.25 mm	6	0.25 mm	125 µm	0.5 mm	35 µm

Table 4.1: Initial dimensions of the novel transformer.

4.2.1 Sensitivity analysis for various design parameters

To compare different design variations of the transformer, one design parameter of table 4.1 is modified independently of the others for which the values in the table are kept. The intent of the design adjustments is to increase k as well as the bandwidth while keeping L_P low. Design recommendations for the IFF method are given at the end of each section. The models in chapter 4.1 are used to point out the changes. The element values are determined by first computing the S-parameters of the structure in the Momentum 3D planar electromagnetic simulator. Afterwards, reactances and resistances are fitted to the S-parameters by a low-frequency RLCk extraction at 500 kHz to create a lumped element model. The resistance and thereby the influence of the skin and proximity effects are neglected for now. Compared to the coupling capacitance, the effect of the interwinding capacitances C_P and C_S is not as significant and therefore the values are not shown either. The relative permittivity of the FR-4 is set to an average value of $\varepsilon_r = 5$ for the simulation [108]. Due to the small outlines it is assumed that the electrical reactance is constant up to f_0.

Width of the secondary winding (W)

Increasing the width of the secondary winding W can reduce the inductance of the secondary winding L_S; see figure 4.3. Since the primary inductance L_P and the mutual inductance L_M are respectively increased and decreased, the coupling coefficient is barely affected. Furthermore, the coupling capacitance C_K is only slightly raised, which is another benefit of the new design.

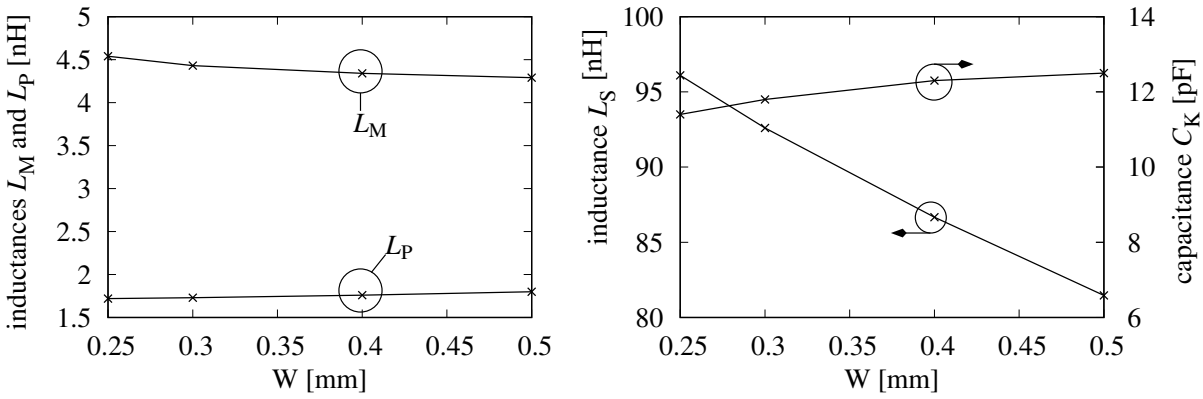


Fig. 4.3: Trend of L_P, L_S, L_M, and C_K with varying diameter of the secondary winding W.

To reduce L_S and thereby increase the bandwidth, the width of the secondary winding **W should be chosen as high as possible** (depending on Y). This is not considering the resistance of the primary winding, since it is ten times smaller than the on resistance of the considered semiconductors and therefore not a critical parameter (e.g. figure 2.5). The maximal considered width is determined

from DD combined with the required annular ring. Increasing W further would reduce the number of secondary turns, since the necessary distances from the vias of the primary winding could not be kept.

Distance between the primary and secondary windings (I)
One of the most important characteristics of the new design is the distance between the primary and secondary windings I. Since the primary and secondary windings are interleaved, increasing the distance I can reduce C_K. Furthermore, the solder resist coat has a significant influence on C_K due to its relative permittivity (e. g. $\varepsilon_r = 3.7$ [109]). Without the coating, C_K can be reduced without changing the inductances L_P, L_S, or L_M. Normally, both parameters are opposing design goals. An example can be seen in figure 4.4. Decreasing the distance I reduces the magnetic leakage flux but increases the capacitance. Thereby, the mutual inductance L_M and thus k is increased while C_K is reduced.

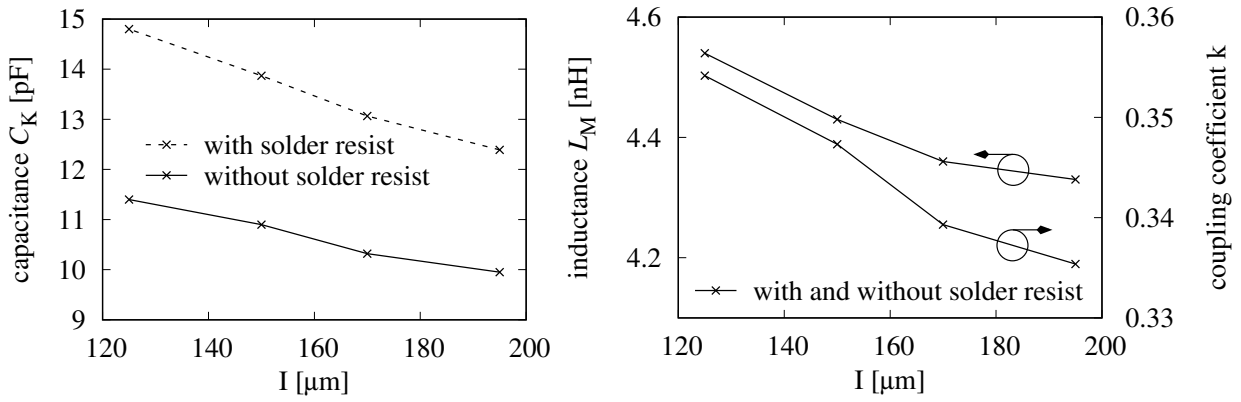


Fig. 4.4: Trend of C_K, L_M, and k with varying distance I between the windings. L_M and k are not affected by solder resist.

To maximize the coupling coefficient, **the distance I should be kept minimal**. Since I defines the isolation between both windings, a minimal width is often necessary. To increase the bandwith **the solder resist can be removed**. This simple adjustment does not affect the other characteristics. Therefore, the simulations of this chapter are done without coating.

Outlines of the primary winding (X,Y)
Increasing the width of the primary winding (Y) is the main design parameter to reduce L_P. To simultaneously maximize k, Y needs to be adjusted to N. By setting the width of each turn or section of the primary and secondary winding DD combined with the additional necessary annular ring, the width of each turn W is 0.6 mm. One primary section/turn is combined with N times a primary section/turn and secondary turn. In combination with the isolation this results in:

$$Y = W + (W * 2 + I * 2) * N = 0.6\,\text{mm} + (0.6\,\text{mm} \cdot 2 + 0.125\,\text{mm} \cdot 2) \cdot 6 = 9.3\,\text{mm}. \quad (4.6)$$

A slightly higher width Y was chosen in table 4.1 to be able to vary I and W, thereby reducing L_P as well as k. Y (and thereby N) could be increased further to reduce L_P, but the width of the utilized semiconductor package would be exceeded. To achieve a compact layout, even for several parallel connected semiconductors, Y was limited to this width.

Since the other design parameters can be set by the application, the length of the primary winding (X) can be used to achieve the necessary mutual inductance. By increasing the overlap area X1 of both windings, the inductance and the capacitance of the transformer can be raised significantly, as can be seen in figure 4.5. But again, the coupling coefficient saturates for a longer transformer.

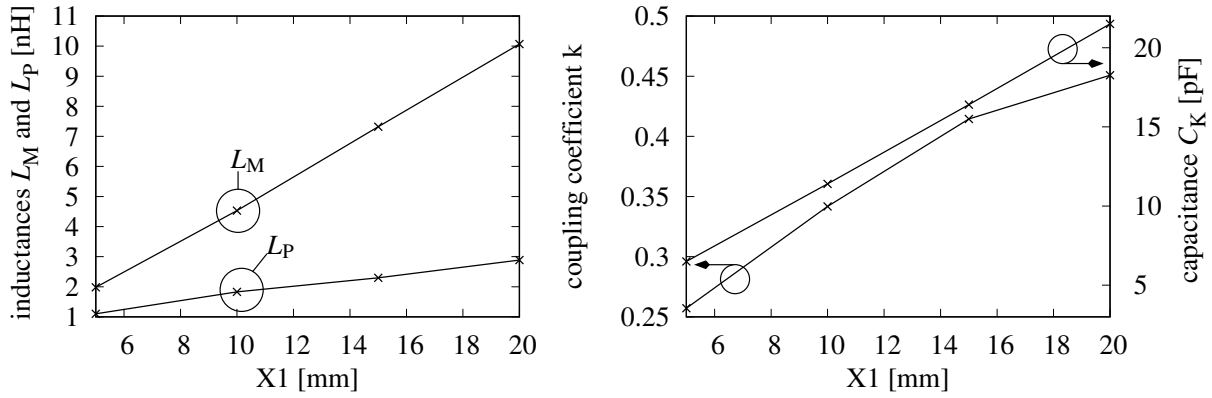


Fig. 4.5: Trend of L_P, L_M, C_K, and k with varying overlap area X1.

Number of secondary turns (N)

A larger number of secondary turns N fitted into the width Y of the primary winding increases the coupling coefficient k significantly by increasing the inductances L_S and L_M. On the other hand, the coupling capacitance C_K is also increased, reducing the bandwidth. The deviation between the approximation of the first resonance frequency f_0 from equation 4.5 and the simulation can be seen in figure 4.6.

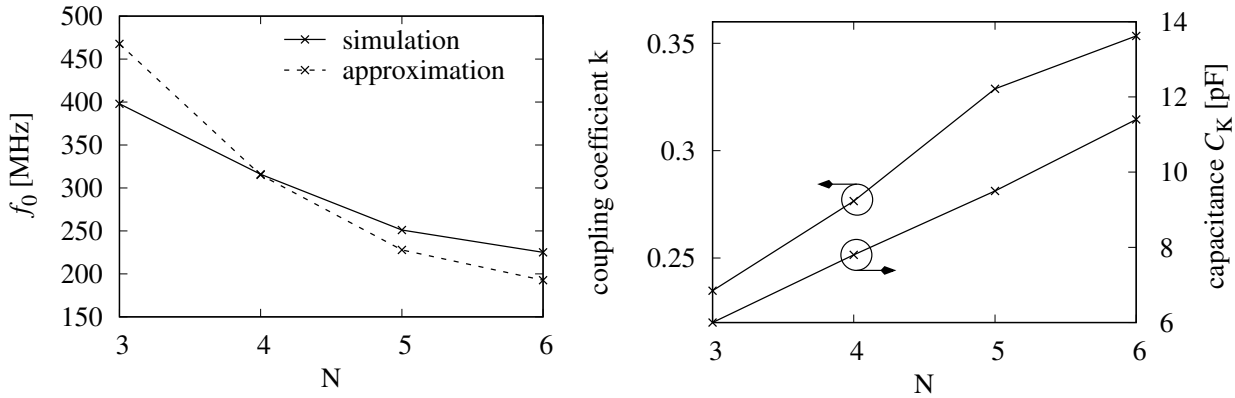


Fig. 4.6: Trend of f_0, C_K, and k with varying number of secondary turns N.

Due to the simplifications of equation 4.3, the approximation should overestimate the influence of C_K, thereby lowering the result for f_0. However, for increasing frequencies, the lumped element approach is less and less suitable. Therefore, for fewer turns, f_0 increases faster in the estimation. This can be recognized by considering the electrical length of the layouts. For four turns, according to equation 2.5 the wavelength at f_0= 315 MHz is 425 mm. With a mechanical length of around 120 mm, the limit of one quarter λ is exceeded significantly for L_S. Therefore, the lumped element approach is not applicable anymore and the bandwidth should be limited by the mechanical length rather than f_0.

To increase the coupling coefficient, the number of secondary turns **N should be chosen as high as possible** (depending on Y). This is because the turns are always enclosed by the primary winding and only the layout restrictions limit the amount of secondary turns.

Thickness of the substrate (Z)

Increasing the thickness of the substrate Z is another way to increase k with only a slight influence on the coupling capacitance C_K (see figure 4.7). This is due to the distance between the vias of the primary and secondary windings V. Increasing the distance can help to decrease C_K further for thick substrate. In this example the approximation of f_0 from equation 4.5 shows the same trend as well as a lower result when compared to the simulation, demonstrating the influence of C_K even though it is overestimated.

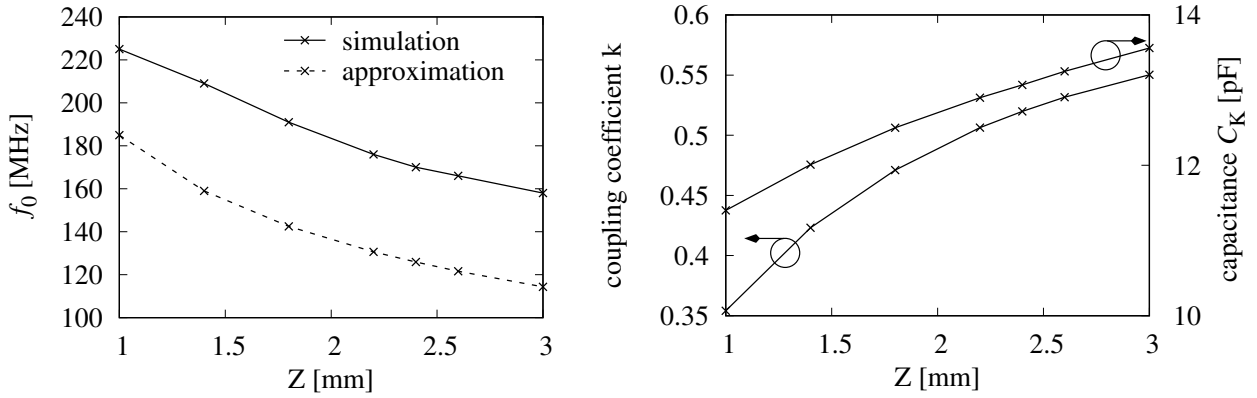
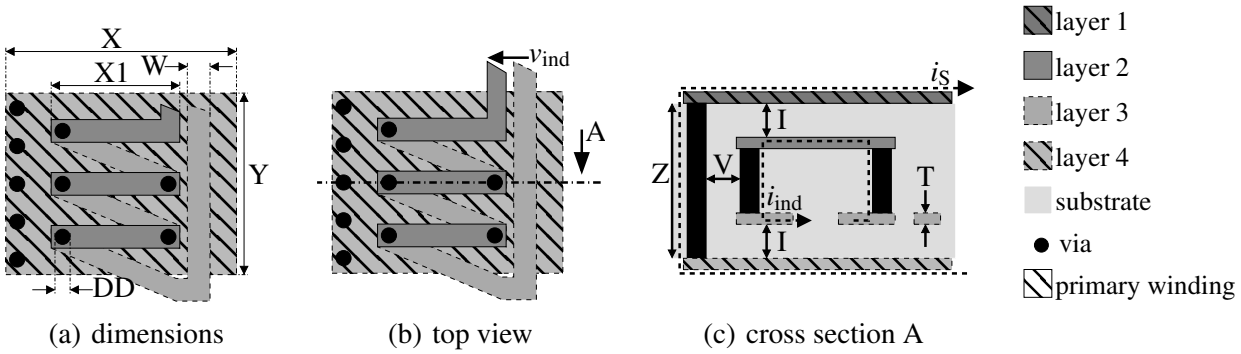


Fig. 4.7: Trend of f_0, C_K, and k with varying substrate thickness Z. A PCB is used in this example.

If the interwinding capacitance becomes critical due to the length X1, reducing the thickness Z can be a solution. Z has only minor influence on L_P and L_S. However, there is again a trade off between the bandwidth and the coupling coefficient. **A thick substrate is beneficial** for a higher k, if the required bandwidth can be achieved.

4.2.2 Reference design of a coreless planar transformer

As a reference, a four-layer design of a coreless planar transformer was chosen as presented in [102]. The figure 4.8(a) shows the dimensions and figure 4.8(b) shows the top view of the layout. To display the inner layers 2 and 3, the top layer 1 was removed. The outlines of layer 1 match the outlines of layer 4. In figure 4.8(c) a cross section of the top view is presented, which includes the source current (i_S) in the primary winding as well as the induced current (i_{ind}) in the secondary winding. Furthermore, the horizontal dimensions are marked. Buried vias are necessary to connect the inner layers, which is still a significant increase in costs for PCB manufactures.



(a) dimensions (b) top view (c) cross section A

Fig. 4.8: Layout of the reference design. To show the encapsulated secondary winding, layer 1 is removed in the top view as well as the dimensions schematic since its outlines match layer 4.

The number of secondary turns N is limited due to the minimal distance and diameter of the vias. Therefore, in a first attempt, the distance I between the primary and secondary windings was reduced in a simulation for a fixed thickness Z of 1 mm. The most important findings can be seen in figure 4.9:

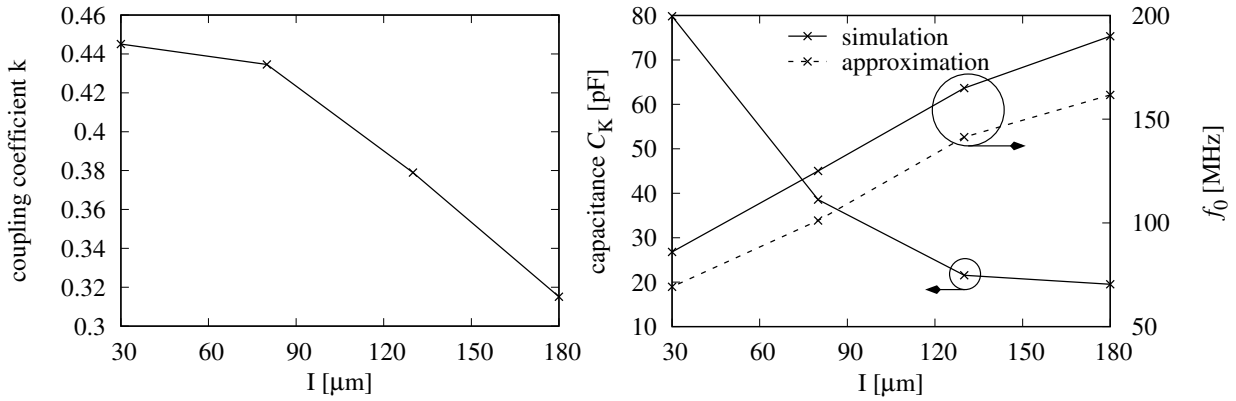


Fig. 4.9: Variation of the distance I between the primary and secondary windings for a fixed PCB thickness of 1mm.

On the one hand, the coupling coefficient k increases significantly since the secondary winding encloses a larger share of the magnetic flux created by the primary winding. On the other hand, the coupling capacitance C_K increases and, thereby, the resonance frequency f_0 is reduced. The deviation between simulated and approximated resonance frequency due to the simplifications in equation 4.3 can be seen. However, the trend is similar. The distance between the primary and secondary windings was limited to I = 130 µm to achieve a high bandwidth and coupling for this four-layer design. To compare the reference design to the novel design in chapter 4.2, similar dimensions are chosen, as can be seen in table 4.2:

X	X1	Y	Z	DD	N	W	I	V	T
13 mm	10 mm	9.5 mm	1 mm	0.25 mm	8	0.25 mm	130 µm	1.3 mm	35 µm

Table 4.2: Initial dimensions of the reference transformer design.

Compared to the novel design, a higher number of secondary turns n could be fitted into the width Y of the primary winding. In exchange, due to an increasing number of opposing vias, a longer distance V was necessary to achieve a comparable trend in capacitance. Furthermore, the length X was increased to achieve a similar inductance of the primary winding L_P for both designs. The PCB thickness was increased to show the influence on the coupling due to an increased enclosed magnetic flux. A comparison of both designs can be seen in figure 4.10. The coupling coefficient k is increased for all considered thicknesses with the four-layer design. This increases with the PCB thickness, due to the higher number of turns and therefore increasing inductances L_M and L_S. On the other side, due to the lack of coating, the coupling capacitance C_K was significantly reduced with the two-layer design. This is especially true for Z = 1 mm due to the additional capacitance between layers 1 and 3 or respectively between layers 2 and 4. Furthermore, the windings in the two-layer design are next to each other and therefore the copper thickness T is more important for the capacitance than the width W.

However, the biggest advantage of the novel design is the simple implementation and easy customization, especially with regard to the distance I, which in a four-layer design is often prescribed by the PCB manufacturer. Since I defines the isolation between the primary and secondary windings, a minimal distance is often required. Nevertheless, due to the big influence of I on the coupling capacitance and coupling coefficient, it should be kept minimal (cf. chapter 4.2.1). To realize a low cost version of the reference design for prototyping, a two-layer PCB can be used for the layout of the secondary winding. The primary winding can than be added through additional copper foil soldered to the PCB [110] or a piece of solid copper [36]. To achieve a high isolation voltage and low distance I, polyimide tape can be used. The relative permittivity of the tape

($\varepsilon_r = 3.6$ [111]) is around the same as that of the solder resist and thus lower than that of the FR4 PCB ($\varepsilon_r = 5$). Still, the capacitance C_K would be significantly higher due to the low distance I, cf. figure 4.9.

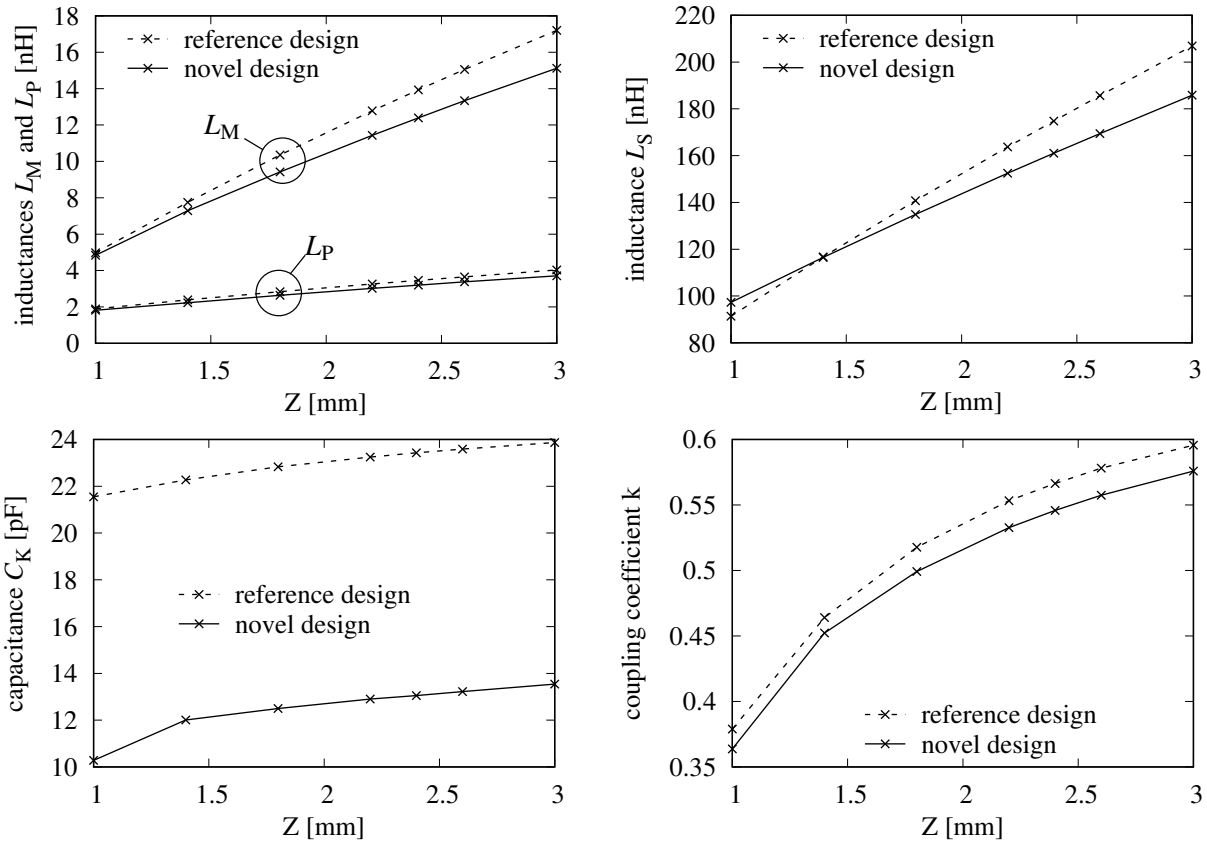
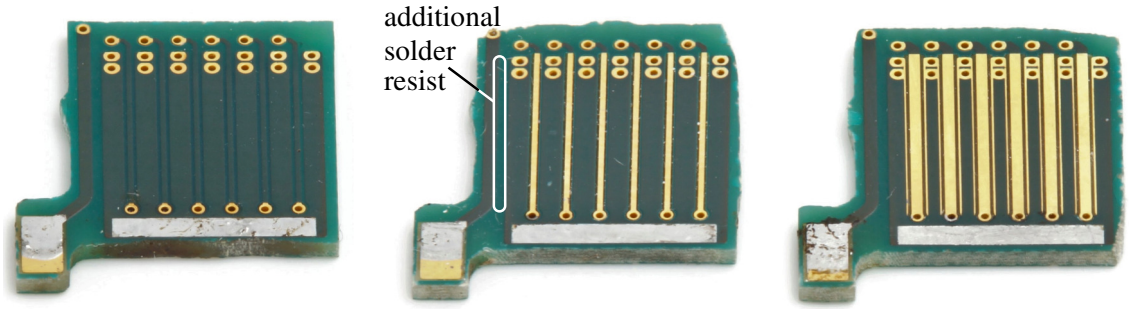


Fig. 4.10: Trend of the lumped elements with varying PCB thickness Z.

The most important argument for the novel design is the higher bandwidth. To give a short comparison, for a thickness Z of 1 mm the reference design achieves around 22 pF which translate to 160 MHz (e.g. figure 4.9). With the 10 pF of the novel design a bandwidth of 220 MHz can be achieved (e.g. figure 4.7). It is important to achieve the required bandwidth and also offer a high coupling coefficient. Overall, the novel design offers a higher bandwidth while achieving comparable electrical parameters for the critical elements. Furthermore, it has less requirements for manufacturing and the critical parameter I is easier to adjust. A benefit from the reference design is the solid primary winding which covers the whole outlines X and Y in copper. Thereby, the resistance of the primary winding could be reduced by the factor two. If the substrate is used for semiconductors with a higher current density than considered in this work, the resistance could become critical. As already mentioned, in this work the resistance of the primary winding is at least ten times smaller than the on resistance of the semiconductors and therefore not a critical parameter (e.g. figure 2.5 and Tab. 4.3).

4.2.3 Characterization of selected layouts

To verify the simulation results of the Momentum 3D planar electromagnetic simulator, three different variations of the two-layer coreless planar transformer were characterized with a VNA. As DUT 1, the basic design of table 4.1 was used with solder resist covering both windings. To demonstrate the influence of the coating, the same layout was used as DUT 2 but the solder resist between the windings was removed. Finally, for DUT 3 in addition to removing the coating, the width of the secondary winding (W) was increased to 0.5 mm. All three variations can be seen in figure 4.11:



(a) DUT 1, W=0.25 mm (b) DUT 2, W=0.25 mm (c) DUT 3, W=0.5 mm

Fig. 4.11: The layouts which have been characterized. The solder resist between the windings was removed in DUT 2 and DUT 3. A small strip of coating was left as marked in the image of DUT 2.

A test fixture was necessary to connect the DUT to the VNA, and this fixture is shown in figure 4.12. The effect of the test fixture on the measurement is de-embedded by a SOLT (short, open, load, through) measurement as in [112]. The smallest possible intermediate frequency bandwidth of 5 Hz was chosen to achieve a high accuracy.

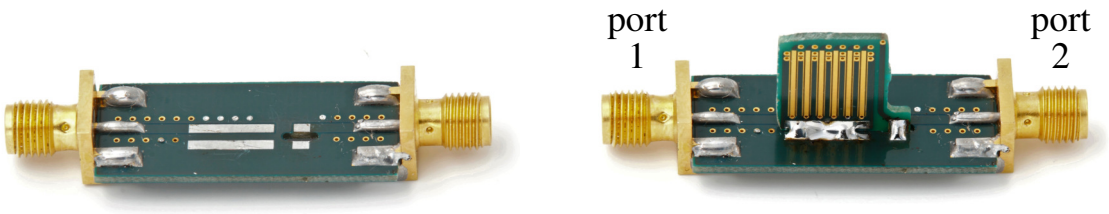
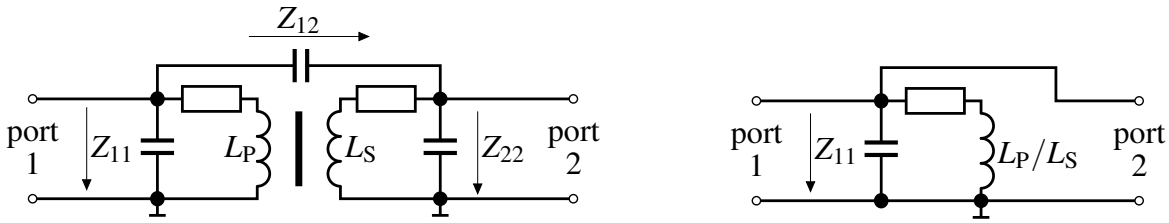


Fig. 4.12: Test fixture without and with DUT connected for a port 1-2 series measurement.

The S-parameters are determined through a port 1-2 series or shunt measurement and then converted into Z-parameters to analyze the results. The two methods can be distinguished by the connection of the DUT to the VNA. The figure 4.13(a) shows a port 1-2 series measurement. The primary winding is connected to port 1 and the secondary winding to port 2 of the VNA. Thereby, all essential elements of the model can be determined. Still, in the considered frequency range, the

impedance has to be greater than 8 Ω to be in the 10 % accuracy range of the VNA. Especially the impedance of the primary winding is significantly smaller in the lower frequency domain.



(a) port 1-2 series (b) port 1-2 shunt

Fig. 4.13: Applied VNA measurement methods.

Therefore, the port 1-2 shunt method can be used to achieve a more accurate measurement. For this method, only one winding is connected to both ports of the VNA, as shown in figure 4.13(b). Thereby, only a fraction of the information about the transformer is obtained.

To illustrate the differences, figure 4.14 shows Z_{11} of a port 1-2 series measurement of DUT 1. For frequencies below 10 MHz, a significant discrepancy between measurement and simulation can be observed, particularly for the phase. This is due to the small impedance of the primary winding.

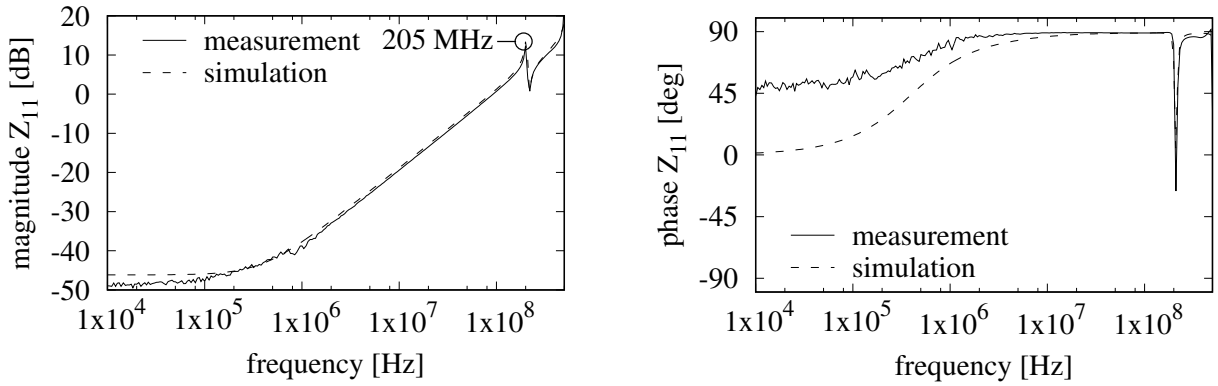


Fig. 4.14: Frequency response of Z_{11} for the port 1-2 series measurement of DUT 1.

By using the port 1-2 shunt method, a sufficient accuracy of the measurement down to around 1 MHz can be achieved. This can again be seen in the phase of Z_{11} in figure 4.15. However, because the secondary winding is left open (in the simulation as well), f_0 increases from 205 MHz to 370 MHz. This is due to the influence of C_K as described in chapter 4.1. Since C_{K1} has no effect during the measurement, the resonance frequency is defined only by C_P. To characterize the whole transformer and to consider the influence of C_K, the port 1-2 series method will be used for the following measurements.

Due to the higher impedance, the port 1-2 series measurement results of the secondary winding

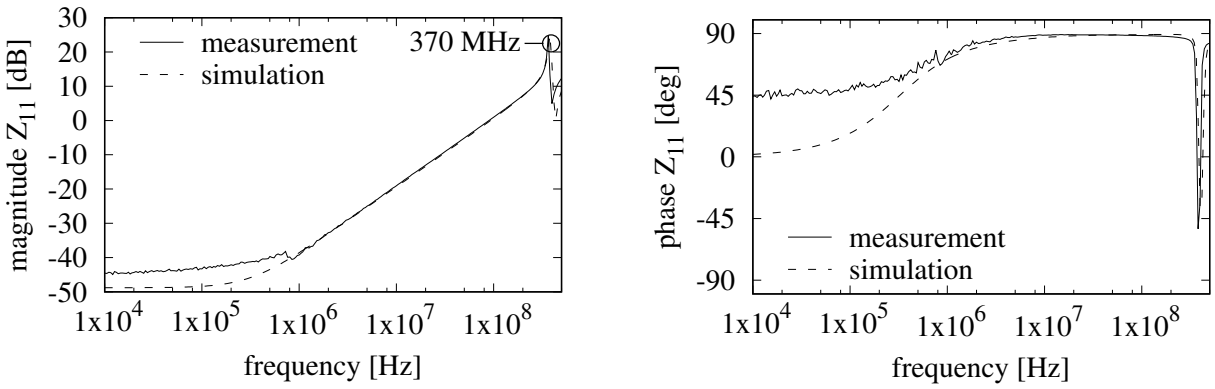


Fig. 4.15: Frequency response of Z_{11} for the port 1-2 shunt measurement of DUT 1.

Z_{22} in figure 4.16 correspond well with the simulation. From 10 MHz to 100 MHz, the phase of around 90° indicates an inductive response of the layout. L_S was therefore calculated from Z_{22} in this frequency domain. Likewise, the inductance of the primary winding L_P can be calculated from Z_{11} and the L_M out of Z_{12}. The results can be seen in figure 4.17.

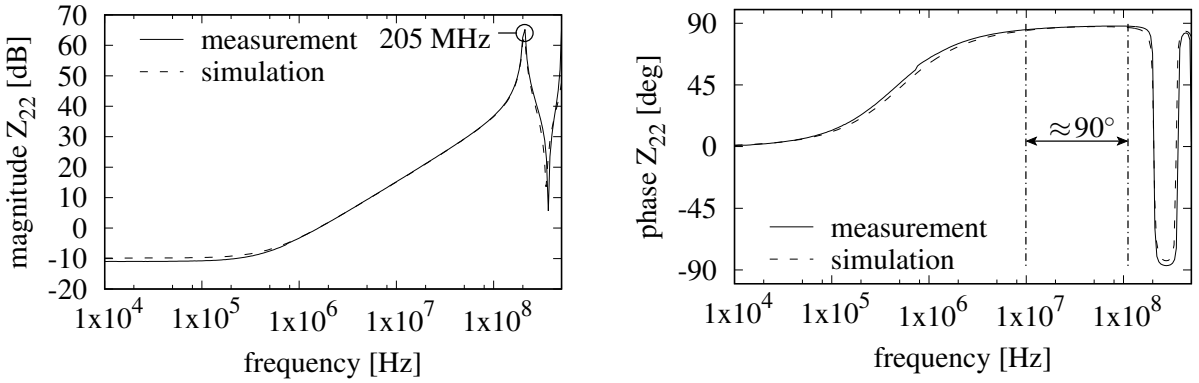


Fig. 4.16: Frequency response of Z_{22} for the port 1-2 series measurement of DUT 1.

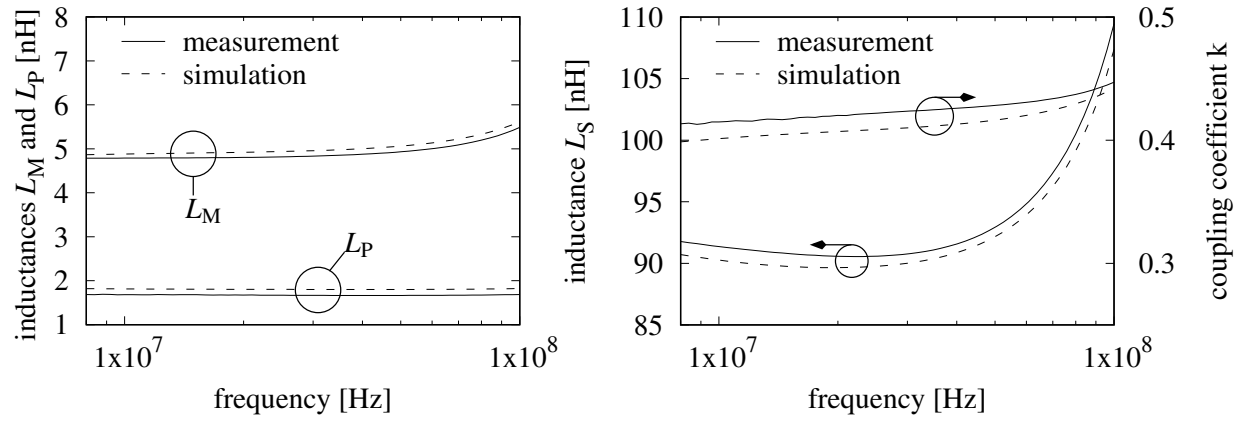
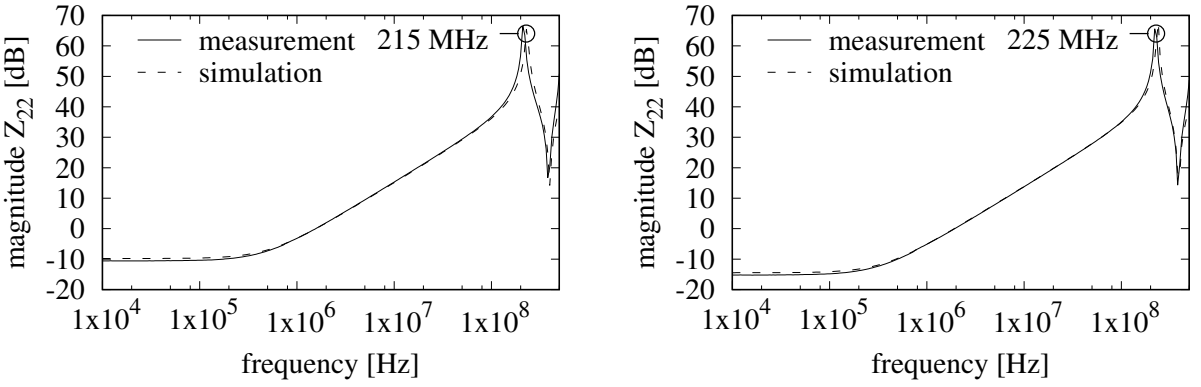


Fig. 4.17: Frequency dependence of L_P, L_S, L_M, and k for DUT 1.

The measurements of all three parameters deviate around 10 % from the simulation. Especially for L_S the limits of the lumped element approach can be seen since the inductance increases significantly with the frequency. The frequency response of the impedance Z_{22} for DUT 2 in figure 4.18(a) shows the advantage of removing the solder resist between the windings. Through this, f_0 was increased from 205 MHz to 215 MHz. The simulation even indicates that f_0 could be raised to 230 MHz if the additional solder resist marked in figure 4.11(b) were removed. For DUT 3 in addition to removing the coating, L_S is reduced by increasing W. Thereby, f_0 was further raised to 225 MHz in figure 4.18(b). By also removing the additional solder resist, f_0 could be increased further to 235 MHz. The frequency-dependent characteristics in figure 4.19 show that L_P and L_M are only slightly affected, as suggested in chapter 4.2.1. Still, the coupling coefficient k of all three designs is comparable. Overall the trends and recommendations given in the previous chapter are validated by the measurement due to the good agreement with the simulation. The results of the RLCk extraction in chapter 4.2.1 for L_S are just slightly lower than the displayed results due to the considered frequency of 500 kHz. This is caused by the frequency dependence of the reactance and will be addressed in the next chapter.



(a) DUT 2, W=0.25 mm (b) DUT 3, W=0.5 mm

Fig. 4.18: Frequency response of the impedance Z_{22} for the port 1-2 series measurement.

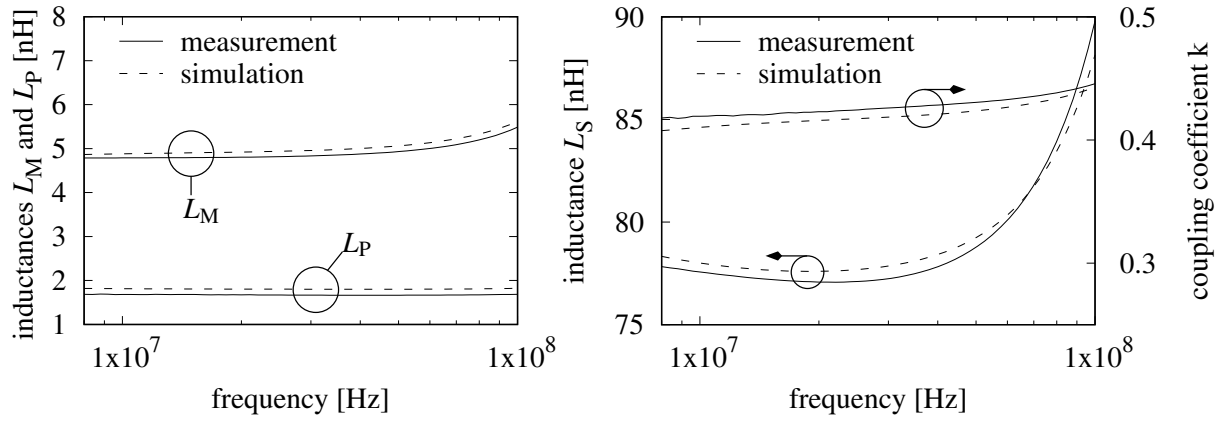


Fig. 4.19: Frequency dependence of L_P, L_S, L_M, and k for DUT 3.

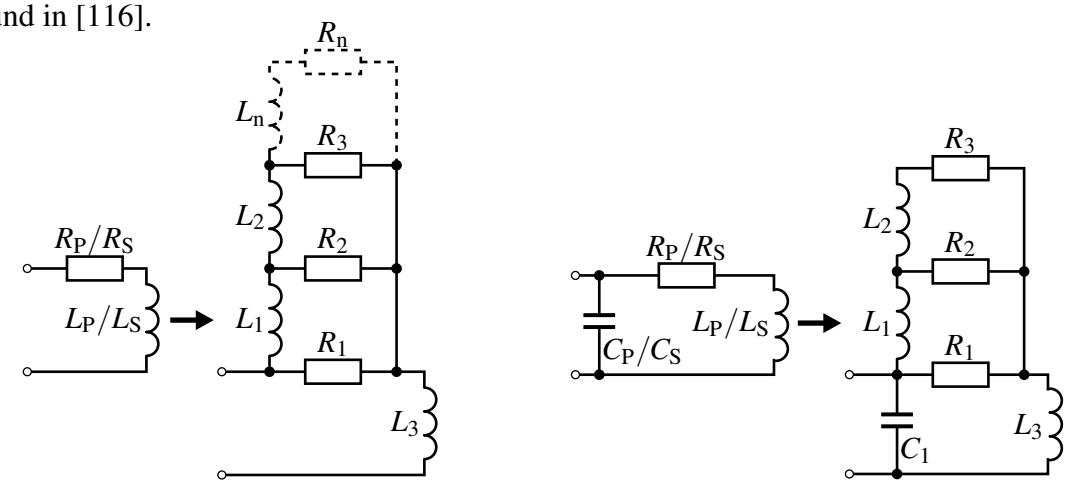
4.2.4 Frequency dependence of the resistance and reactance

Up to now the frequency dependence, especially of the resistance, has been ignored. Thus, the frequency response of DUT 1 from chapter 4.2.3 is further analyzed. Thus far the lumped element model introduced in chapter 4.1 has been applied. The parameters of DUT 1 corresponding to this basic model can be found in Tab. 4.3.

L_P	L_S	L_M	C_P	C_S	C_K	R_P	R_S
1.7 nH	96 nH	4.54 nH	7.9 pF	6.7 pF	14.8 pF	5 mΩ	322 mΩ

Table 4.3: Simulated parameters of DUT 1 in accordance with figure 4.1(a).

However, eddy currents have a significant influence in the considered frequency range. Therefore, the previous lumped element model has to be extended to cover the skin and proximity effects. To ensure that the model can be used in a conventional SPICE simulator, a solution based on frequency independent elements was favored. To illustrate the skin effect, [113] proposes an R-L ladder structure as shown in figure 4.20(a). At DC the impedance of the R-L network is equal to the parallel connected resistances and increases with frequency up to a maximum resistance R_1. A compact version with only one additional R-L structure is presented in [114]. A higher accuracy can be achieved by increasing the R-L count. [115] recommends increasing the resistance and inductance between each R-L structure on the basis of a square-law relationship. As a result, high accuracy can be combined with a low R-L count. For this work two additional R-L structures provide a sufficient accuracy in the essential frequency range up to f_0. Instead of calculating the skin depth to obtain the model parameters, the model was fitted to the Momentum simulation results to also cover the proximity effect. This was achieved by minimizing the least square error between model M1 or M2 of figure 4.20 and the simulation results. A comparable approach can be found in [116].



(a) model M1 (b) model M2

Fig. 4.20: Models realizing frequency dependent resistance and reactance.

In figure 4.21 a comparison between the simulation and measurement of the primary winding of DUT 1 can be seen. This is the initial dataset used for the fitting. For both models M1 and M2, it is important that only the interwinding capacitance C_P or C_S is considered for the fitting of C_1 (which should match C_P/C_S). Therefore, the measurement and simulation results from the port 1-2 shunt measurement of DUT 1 are utilized. Otherwise, the coupling capacitance C_{K1} (compare figure 4.1(b)) would also be taken into account for the fitting of C_1, thereby falsifying the model.

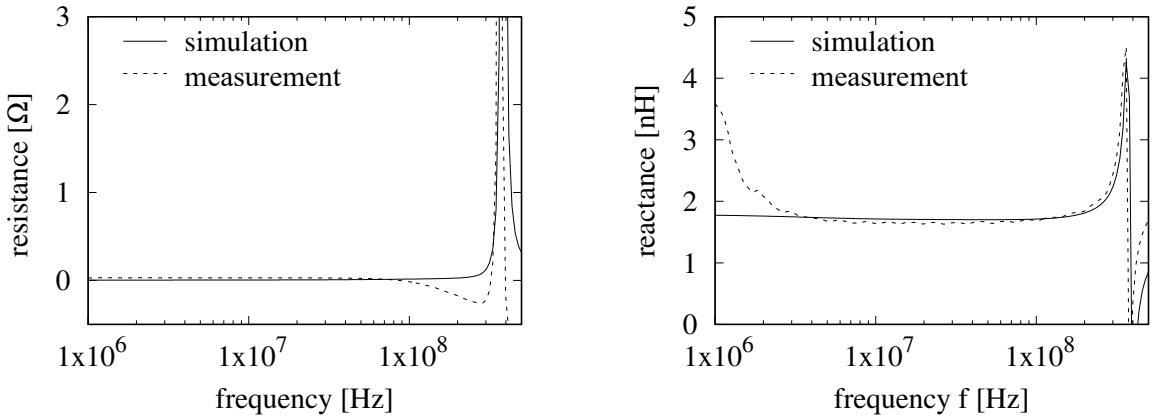


Fig. 4.21: Frequency response of the primary winding of DUT 1.

However, the simulation results show that up to first resonance frequency (f_0) of 205 MHz, the resistance and reactance part are constant for the primary winding. There is a deviation of the measurement above 100 MHz which is probably due to the impedance of the short standard necessary for the de-embedding of the test fixture. The standard is not an ideal short and starts to have a noticeable influence on the measured resistance. Still, in the considered frequency domain, a frequency dependent model is unnecessary for the primary winding. Because of the small width W, eddy currents have a greater influence on the secondary winding of DUT 1. Particularly the resistance in figure 4.22 rises significantly close to f_0. But even the reactance is affected above 2 MHz.

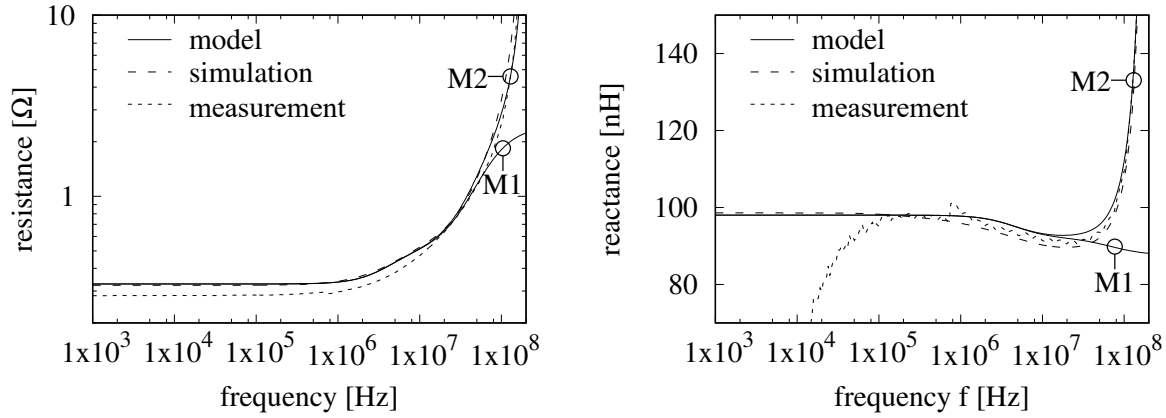


Fig. 4.22: Frequency response of the secondary winding compared to model M1 and M2.

Below 100 kHz even the port 1-2 shunt measurement is too inaccurate and should be disregarded. Therefore, the models M1 and M2 are fitted to the simulation results. As can be seen in figure 4.22, model M1 is accurate only for frequencies up to around 50 MHz. If the transformer should be modeled up to the first resonance frequency, the interwinding capacitance cannot be neglected and model M2 is necessary. Overall, with the two additional R-L structures, an accurate fit to the frequency response is possible.

By combining the initial lumped element model with the model M2, a high accuracy of the simulation up to f_0 can be achieved. The resulting simulation circuit in figure 4.23 consist merely of passive components. Accordingly, it is suitable for conventional SPICE simulations. The calculated parameters of the final model for DUT 1 can be found in table 4.4.

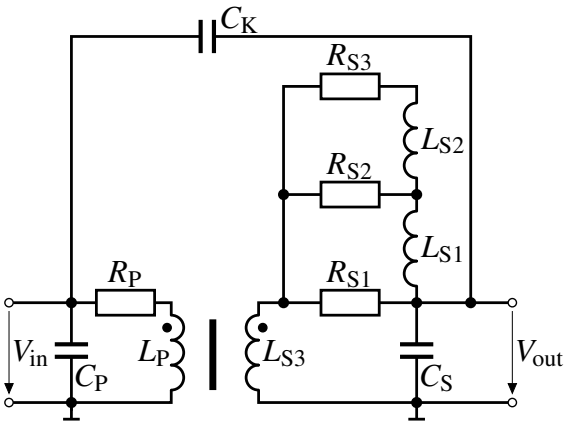


Fig. 4.23: Final simulation model of the coreless planar transformer.

L_P	k_{PS3}	L_{S3}	L_{S2}	L_{S1}	R_P	R_{S1}	R_{S2}	R_{S3}	C_P	C_S	C_K
1.7 nH	0.37	88 nH	51 nH	7 nH	5 mΩ	2.45 Ω	0.6 Ω	1 Ω	7.9 pF	6.7 pF	15 p

Table 4.4: Model parameters for DUT 1 of the coreless planar transformer.

5 Current sensor application

Even though the main goal was to achieve an improved design for the IFF method, the coreless planar transformer is also suitable for further applications. In this chapter the design will be used as a Rogowski coil to realize a current sensor optimized for half bridge circuits. Current sensors are classified into two types: non-isolated resistive sensors based on Ohm's law and isolated sensors that evaluate the electromagnetic field. The disadvantages of resistive sensors in high current applications are power losses, which reduce system efficiency, and susceptibility to over-current, which can damage the sensor. The minimal feasible resistance is regularly limited by the accuracy or additional amplification, which reduces the bandwidth and increases the sensor's complexity. For MOSFETs, a current mirror can be the solution to provide an equivalent current path with a reduced amplitude [117].

Isolated current sensors, on the other hand, are a more universal solution with the additional advantage of enabling the measuring circuit to be added to a different voltage class. Three different principles are typically used to realize an isolated current sensor [118]: By determining the Faraday effect, an optical fiber can be used to measure the current. The advantages of this measurement approach are immunity to electromagnetic interference, lightweight, high sensitivity as well as a large bandwidth [119]. Anyhow, bending stress of the fiber optic cable must be prevented which limits the possible stress. Furthermore, the high complexity and space requirements go against the introducing of a fiber optic sensor into a half bridge circuit.

Another group of current sensors measure the magnetic field and thereby deduce the associated current. Examples are sensors based on magneto resistive materials or the hall effect and fluxgate sensors. A benefit of these sensors is, that they can detect both static and dynamic magnetic fields, allowing them to measure direct and alternating currents. However, the application can be complex in compact designs because a good positioning is important to exclude interfering fields. Furthermore, to determine the relationship between the magnetic field and the current, the sensor must be tuned.

Finally, also Faraday's law of induction can be used to measure an alternating current: The induced voltage in the secondary winding of a transformer is proportional to the rate of change of the current in the primary winding. A current transformer uses a core material with high relative permeability to achieve a good coupling and realize a high accuracy in the selected measurement range. A modification of the current transformer is the Rogowski coil. Since there is no magnetic material used to couple the windings, saturation due to high currents is not critical. Therefore, a linear output can be achieved for a wide measurement range.

Modern semiconductor packages reduce their stray inductance by removing the leads as in a dual-flat no-leads (DFN) package. Comparable designs are also available for power semiconductors [55, 61, 68]. Another approach which is currently investigated is to integrate the bare dies into the PCB [120]. Conventional Rogowski coils are clipped around a conductor [121] and thus can hardly be added to these current commutation loops. Nevertheless, the high bandwidth and isolation are a perfect match for the increasing slew rates and voltage range of modern semiconductors. Because of this, the Rogowski principle is applied to an additional component that is soldered to the PCB [122] or integrated into the PCB [102]. A main characteristic of these designs is how much inductance they add to the commutation loop. It is for this reason that the novel design is particularly suitable for a current measurement integrated into the commutation loop.

Conventional Rogowski coils are often used with galvanic isolation. Then, the capacitive coupling is negligibly small and therefore not considered for determining the transfer characteristics [107]. The use of the novel design as a Rogowski coil is limited by the first resonance frequency f_0. The current in the secondary winding i_{ind} is increased significantly around f_0 and therefore f_0 limits the bandwidth up to which V_{out} of the Rogowski coil has a direct reference to i_{S} (cf. equation 4.2). As described in chapter 4.2.1, most of the adjustable parameters in the novel design, such as the number of secondary turns N or the thickness of the substrate Z, cause a trade-off between f_0 and k. Therefore, if a higher bandwidth is required, V_{out} is reduced due to a lower mutual inductance. Especially if the design goal is to achieve a low primary inductance, sufficient amplification is necessary. Particularly the low frequency domain requires a high gain because of the low impedance of the transformer.

5.1 Signal conditioning circuit

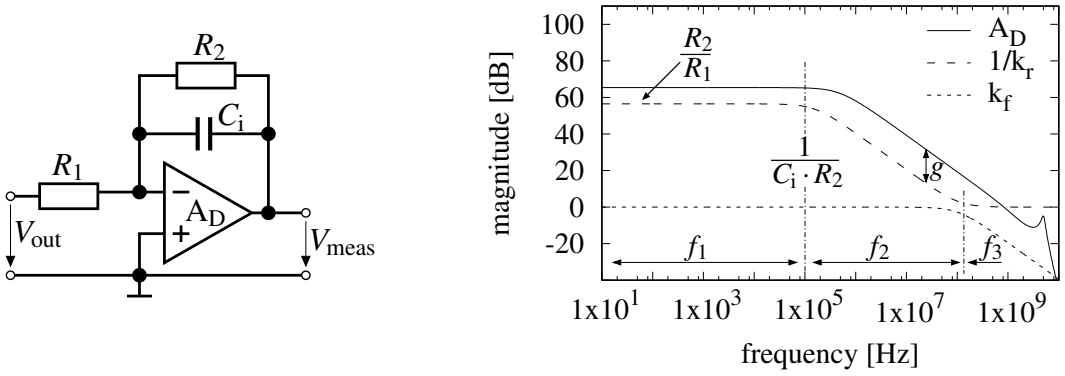
Since the Rogowski coil measures the time derivative of the current, the output has to be integrated. Due to offset voltages and biases, an integration error occurs and complex digital postprocessing with calibration and offset correction can be necessary [123]. However, in this chapter a simple integrator circuit based on an operational amplifier as shown in figure 5.1(a) will be used to instantaneously get a representation of the current waveform. Generally, the closed loop gain A of a operational amplifier, which is equivalent to its transfer function, can be described by:

$$A = k_\mathrm{f} \cdot \frac{A_\mathrm{D}}{1 + k_\mathrm{r} A_\mathrm{D}} \quad \text{where} \quad k_\mathrm{r} A_\mathrm{D} = g. \tag{5.1}$$

Therefore, the transfer function includes the open loop gain A_D as well as the preamplification k_f and feedback factor k_r [124, p. 488]. To achieve a linear frequency response over a wide frequency range, the loop gain g has to be high enough to make sure that:

$$A \approx \frac{k_\mathrm{f}}{k_\mathrm{r}} \quad \text{if} \quad g \gg 1. \tag{5.2}$$

The reciprocal value of g is therefore also known as computation accuracy. The magnitude of all three proportions of A is displayed in figure 5.1(b) for a reference integrator setup (cf. [124, p. 732]). Due to the logarithmic scale, g is equal to the difference of A_D and $1/k_\mathrm{r}$. The frequency response can be split in three different frequency domains. During f_1 the circuit only amplifies the signal due to a constant gain. Only for higher frequencies does the circuit integrate the input signal. Therefore, a lower frequency limit can be found around $1/(C_\mathrm{i} \cdot R_2)$. To avoid high noise in the lower frequency domain and to make sure that g is already high enough at the lower frequency limit, the magnitude of $1/k_\mathrm{r}$ in f_1 should be lower than A_D.



(a) equivalent circuit (b) frequency response of the loop gain

Fig. 5.1: Design of the utilized integrator.

Therefore, a trade-off between computation accuracy and gain is required. During f_2, A corresponds to $1/k_r$ since k_f is 0 dB. Similarly, during f_3, A corresponds to k_f. However, since g is reduced continuously for increasing frequencies in this frequency domain, the condition of equation 5.2 becomes invalid, creating an upper frequency limit. Furthermore, the upper frequency limit becomes similar to the transition between f_2 and f_3 for high frequencies, since the ideal low pass characteristics are difficult to achieve with actual components in combination with the inductances added by the PCB.

Nevertheless, the computation accuracy of the upper frequency limit is based solely on A_D, which makes a high gain bandwidth product vital. Bipolar amplifiers normally offer a high gain bandwidth product. Still, a CMOS operational amplifier was favored over a bipolar input to reduce the integration error due to the bias current. Even though an decompensated operational amplifier would also offer a higher gain bandwidth product, it was excluded to avoid instabilities. The design goal was an upper frequency limit of around 200 MHz, which fits the current transition time realized by the IFF method. A computation accuracy of around 15% is achieved at the upper frequency limit.

5.2 Characterization of the current sensor

A full schematic of the final current sensor model can be seen in figure 5.2. It is divided in four different blocks. At the input a simplified model of the coreless planar transformer as in figure 4.1(a) is used, neglecting the skin and proximity effects. The mechanical dimensions are as shown in table 4.1 except for X1 = 5 mm. After the transformer, the components of the signal conditioning circuitry are added, beginning with a passive low pass filter introduced to dampen the first resonance frequency of the transformer. The filter is followed by the integrator and finally a voltage divider, which is necessary if the chosen amplifier is driving a 50 Ω input.

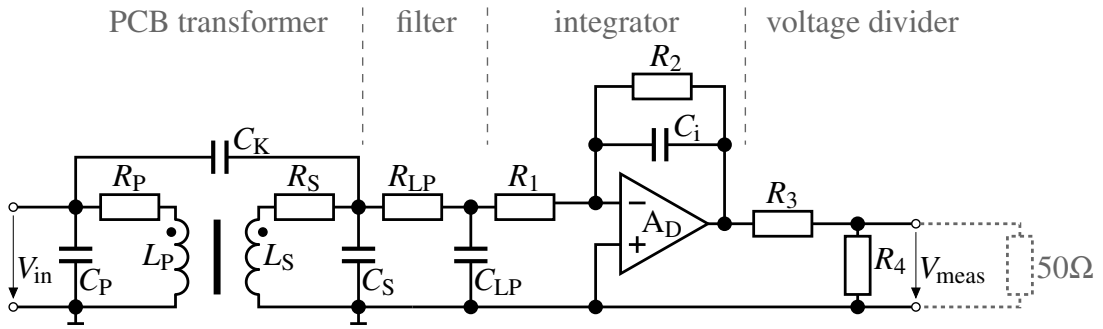


Fig. 5.2: Final simulation model of the current sensor.

The practical realization also uses a potentiometer at the positive input of the amplifier to adjust the offset of the measurement voltage V_{meas}. A picture of the populated PCB can be seen in figure 5.3. The corresponding model parameters can be found in appendix chapter A.1.

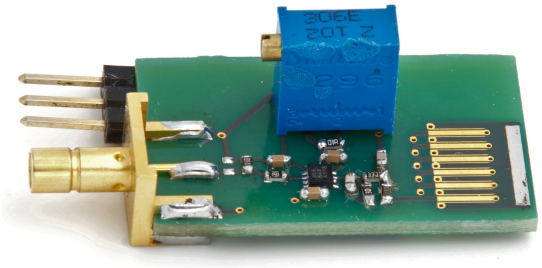


Fig. 5.3: Implementation of the current sensor, using the coreless transformer as a Rogowski coil.

The forward voltage gain of the current sensor can be seen in figure 5.4. An additional 50 Ω resistor in series with the input was necessary to achieve the 10 % accuracy range of the VNA. The discrepancies between measurements and simulation, particularly in the higher frequency domain, are based on the ideal simulation model. The influence of the PCB was ignored and especially the tolerances of the integration capacitance C_{i} can have a significant influence on the magnitude. The phase shift has to be taken into account when measuring in the according frequency domain, it can especially influence measurements in the lower frequency domain.

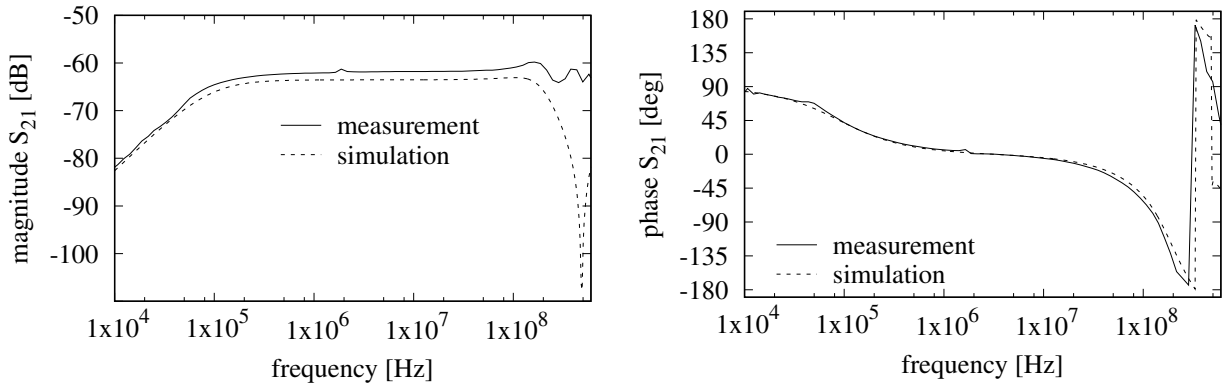


Fig. 5.4: Forward voltage gain of the current sensor.

The output of the signal conditioning circuitry V_{meas} is designed to accurately represent the measured current, especially at high current gradients. To qualify the accuracy of the final current sensor, it was compared to a reference sensor with a bandwidth of 200 MHz [125]. The output of both sensors can be seen in figure 5.5. A current transition from 0 A to 1.1 A with a transition time of 3 ns was used as a test signal. To achieve this a signal generator was combined with an amplifier and thereby limiting the bandwidth to 250 MHz.

For the first 40 ns, the measurement results of the current sensor show good agreement with the

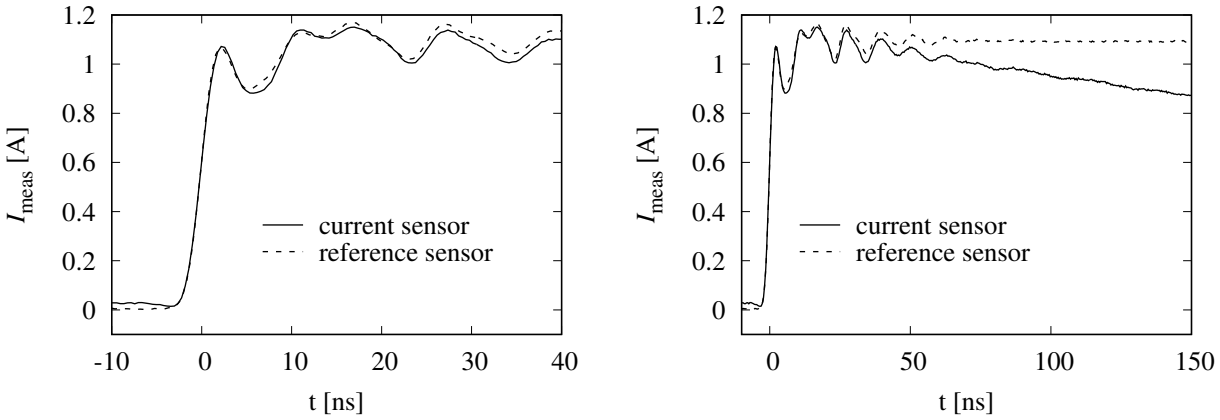


Fig. 5.5: Comparison of a measured current slope with a 200 MHz reference sensor.

reference sensor. The discharging of C_i due to R_2 leads to an output voltage drift for an extended time period. However, in an ideal integrator circuit, an input offset would also result in an output voltage drift over time until the operational amplifier saturates. In power inverters, resetting the ideal integrator circuit can be sufficient [126] and even the DC component of the load current can be calculated from the currents in both DC link terminals [127]. Normally, the Rogowski coil is combined with an additional sensor (e.g. tunnel magnetoresistance [128] or Hall effect [129]) if measuring from DC up to a certain cut-off frequency is necessary. A further improvement of the sensor would be to reduce the noise of the lower frequency range, for example, with an additional feedback network that dampens only the frequencies below the lower frequency limit of the integrator circuit [130]. Using an amplifier as the low pass filter could further reduce the phase error in the upper frequency range. As pointed out, various improvements of the current sensor are possible. Nevertheless, for the intended purpose of measuring the current slope of the IFF method, the bandwidth is sufficient.

6 Improved inductive feed forward

In this chapter the novel design of a coreless planar transformer will be used to improve the inductive feed-forward method. Different power semiconductors will be utilized and if necessary, modifications are presented. Unless otherwise stated, a double pulse circuit, as introduced in chapter 3.1.1, is used to characterize the different concepts with an adjustable load current (I_L). Often, only the gate loop is shown in the following for clarity. To ensure comparability of the measurements, all circuits are analyzed switching a voltage of V_{sup} = 400 V with a fixed L_{DP} and D_{FWD}. Since the focus of the modifications will be the gate loop, the schematic will be simplified by leaving out L_{DP}, D_{FWD}, and V_{sup}. Of course these elements are still present in the measurement setup. As a result, it becomes apparent that the different approaches can be used in various power converter topologies. Explicit values for the critical components used in the different circuits can be found in the appendix. The PCBs of the different test setups also have a comparable design. As an example, in figure 6.1 a PCB designated for a double pulse measurement can be seen. A complete commutation cell is included and different gate driving methods can be selected. T_{FF} can be added right underneath the semiconductor to realize the IFF method. The connections of T_{FF} to the gate are parallel to R_G, which has to be moved for the IFF method. This way, the IFF method can be compared to the conventional approach with small changes to the same setup, allowing for minimal stray inductance of the source loop when T_{FF} is replaced by a jumper. An optical control of the gate driver as well as an isolated voltage supply ensure that i_{SM} can be used to determine the switching losses.

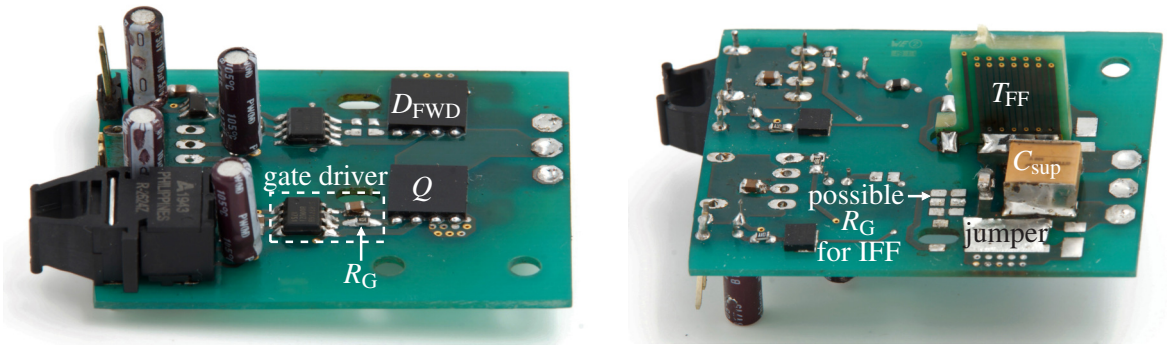
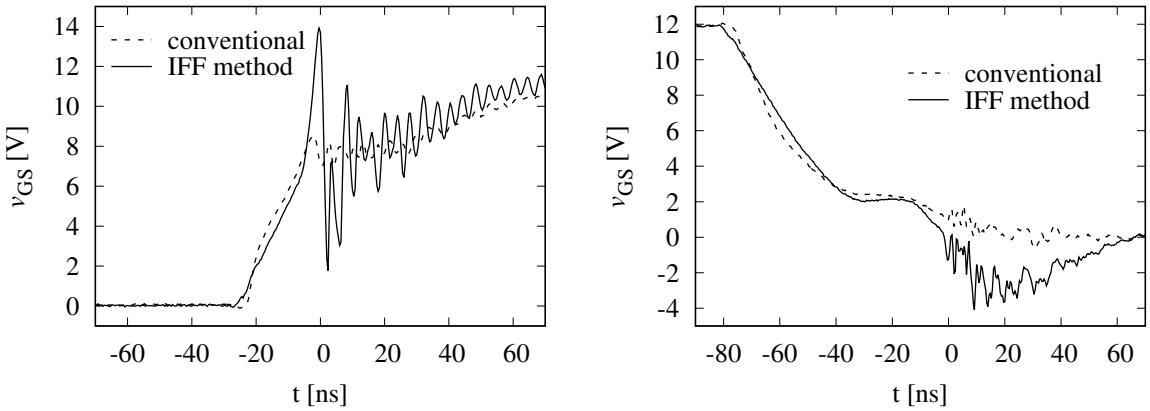


Fig. 6.1: Top and bottom view of a PCB for a double pulse measurement using a SJMOSFET.

6.1 Application to superjunction MOSFETs

The SPICE simulations in chapter 3.2 have already shown the main advantages and characteristics of the IFF method. In this chapter, the simulations will be verified by measurements to show the actual acceleration of the transitions by the IFF method and the limits of the simulation. Again, the conventional approach with a single resistor in series with the gate is compared to the IFF method with the additional transformer T_{FF} (cf. figure 3.4). A modern 600 V Si SJMOSFET was used as semiconductor and a typical positive gate voltage of 12 V was chosen. The most distinguishing feature, the v_{GS} trend, is compared in figure 6.2 for the turn-on transition in the left plot and the turn-off transition in the right plot.



(a) turn-on transition (b) turn-off transition

Fig. 6.2: Comparison of the gate-source voltage of the SJMOSFET turning on and off I_L= 15 A.

For the conventional approach, during turn on the gate voltage rises to only 7 V and then stagnates until rising with a reduced velocity. Since the SJMOSFET is equipped with a Kelvin contact the first presumption is to explain the plateau exclusively with the voltage-dependent gate capacitance, see [131]. The capacitance increases during the transition, limiting the voltage rise due to the gate resistance. However, the nonlinear capacitance of recent SJMOSFET amplifies the impact of the common source inductance [132]. Thus, even with a Kelvin contact an influence of the remaining inductance is possible.

The IFF method on the other hand adds an additional voltage to the gate during turn on. The higher voltage due to the transformer T_{FF} can be seen just before the voltage transition at 0 ns. Afterwards, the gate voltage shows an oscillation due to the additional inductance added by the transformer and the stimulation by the IFF method. The maximum v_{GS} is 14 V, leaving a safety margin to the maximum gate voltage of the device. For this semiconductor, a maximum dynamic gate-source

voltage of 30 V for frequencies above 1 Hz is specified. Therefore, further increasing v_{ind} for an additional acceleration would be possible. The maximum v_{GS} also differs significantly to the simulations in figure 3.7, probably because of several reasons. In contrast to the transformer T_{FF}, the skin effect was not considered in the simulations of the main PCB in figure 6.1. Furthermore, in the simulation the gate driver is replaced with a simple voltage supply with an ideal resistance. Both measures ignore the frequency dependency of the components, which explains the additional damping and the lower ringing in the measurements (cf. chapter 4.2.4).

For turn off, the influence of the additional transformer T_{FF} on the gate-source voltage is modest. Due to the decreasing source current, a negative voltage is added to the gate which is clearly visible in the comparison. This time the actual voltage is much lower than in the simulation and the additional oscillation can be neglected. Probably because of the higher damping due to the skin effect, the current gradient is not as high during turn off. In addition, the current is not forced by L_{DP} as during turn on. The maximum negative dynamic gate-source voltage is easily met and even asynchronous $V_{\mathrm{GS,max,dyn}}$ limits as for SiC devices should not be problematic (cf. chapter 2.1.2).

To get a comprehensive overview about the switching characteristics, the voltage v_{DS} as well as the current in the semiconductor is essential. As explained in chapter 3.1.1, the i_{SM} is measured because of the lower isolation requirements and easier connection of the measurement setup to the power loop. The current sensor from chapter 5 is used for this purpose. In figure 6.3 a comparison of the turn-on transition can be seen.

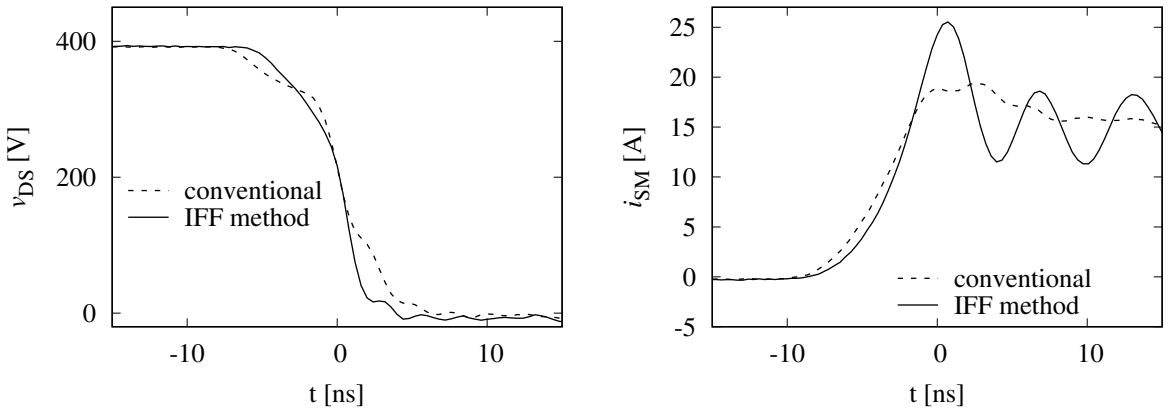


Fig. 6.3: Comparison of v_{DS} and i_{SM} of a SJMOSFET turning on $\mathrm{I_L}$= 15 A.

The basic differences between the conventional and the IFF method can again be found in the measurement and are as in the simulation. The current gradient increases continuously for the IFF method, creating a higher peak current and ringing. The v_{DS} slope is rounded and the highest slew rate is achieved in the end of the transition. The conventional approach on the other hand, shows almost constant current gradient for the most part and a much lower peak current. An

additional lower voltage drop can be seen before the main v_{DS} drop with the highest slew rates follows up. In contrast to the simulation, the transition of the conventional approach seems to be briefly interrupted during the transition at around zero ns (cf. figure 3.6). Overall, the short interruption seems to compensate the lower peak current. The turn-on losses in figure 6.4 only differ slightly from the simulation in figure 3.9(a). The reduction of the switching losses as well as the moderate increase of the IFF method in contrast to the conventional approach is clearly visible. At the maximum continuous drain current of 14 A, for the conventional approach $E_{\text{turn-on}}$ is around 42 µJ. The IFF method achieves an $E_{\text{turn-on}}$ 32 µJ which is a reduction by 24 %.

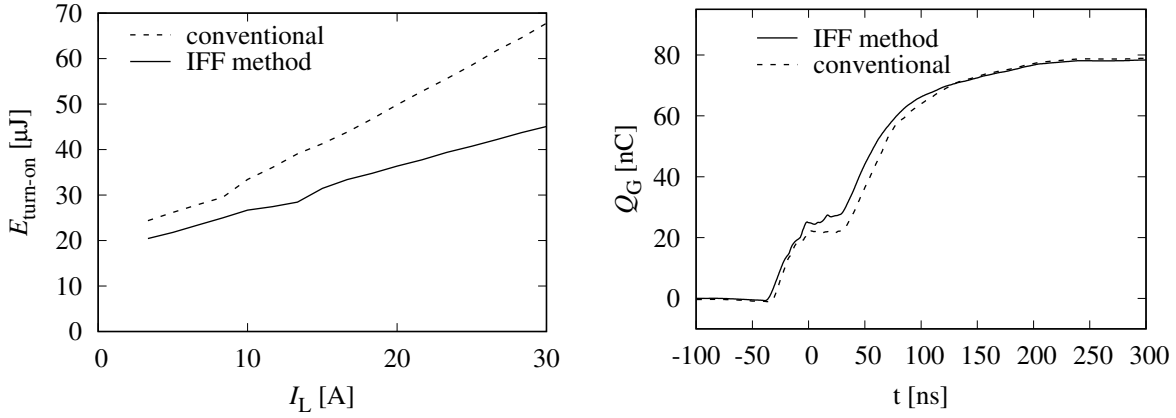


Fig. 6.4: Turn-on losses for varying load currents and charging of the gate for I_L= 15 A.

The reduction of the turn-on losses can also be explained by the course of the gate charge measured by integrating the current through the gate resistor. Due to the IFF method the gate is charged faster during the transition at 0 ns compared to the conventional approach. Instead of an almost constant gate charge during the miller plateau phase, the charge is still increasing, shortening the transition. The simulation, even though it is simplified, resulted in a realistic estimation of the loss reduction during turn on.

For the turn-off losses the accuracy of the simulation still has to be verified. In figure 6.5 a comparison of the turn-off switching characteristics can be seen. The IFF method shows a similar behavior as the conventional approach. This is contradicting the simulation in figure 3.8, where a higher slew rate is achieved with the IFF method. An explanation was already given for v_{GS}, where the voltage drop is significantly reduced. Contrary to the turn-on transition where the current gradient increases continuously, an almost constant current gradient during turn off is created by the IFF method.

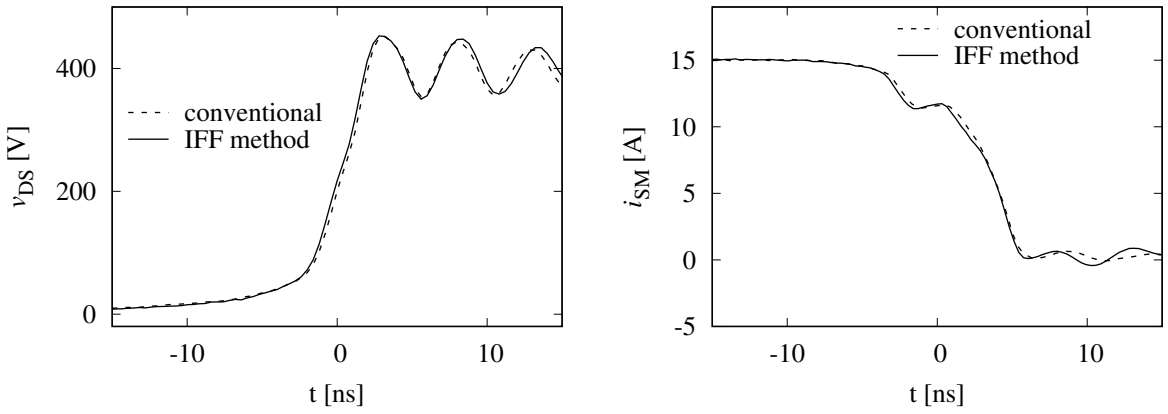


Fig. 6.5: Comparison of v_{DS} and i_{SM} of a SJMOSFET turning off I_L= 15 A.

The turn-off losses in figure 6.6 show a similar progression of both methods up to around 20 A. Only for higher load currents, $E_{\text{turn-off}}$ is slightly reduced by the IFF method. An indication for the different trends can also be found by examining $V_{DS,max}$. The voltage is comparable up to around 20 A. Only for higher load currents, the voltage differs with the IFF method showing a mostly higher peak voltage. This is the same distinction the simulation showed between both methods, even though for the measurement a significant higher load current was necessary. Overall, the IFF method does not offer any advantages in the current range up to the maximum continuous drain current of 14 A. The simulation is misleading due to the frequency dependence of the PCB which is excluded, resulting in higher ringing and current gradients as in the measurements.

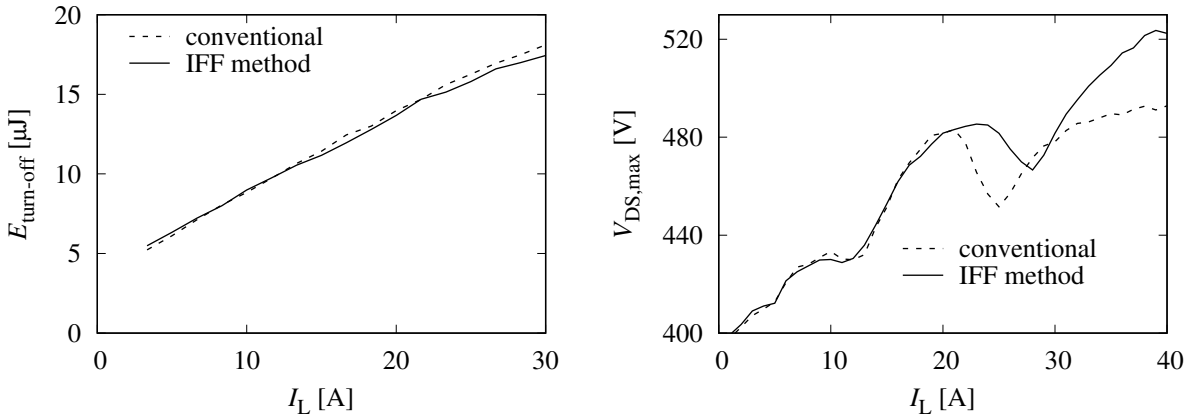


Fig. 6.6: Turn-off losses and the maximum drain-source voltage for varying load currents.

Even though the IFF method has not shown benefits for the turn-off losses of the SJMOSFET, a lower $C_{O(ER)}$ and higher current gradients could reduce the load current above which it has an influence on the $E_{\text{turn-off}}$. SiC power semiconductor therefore seem to be more suitable to assess the suitability of the IFF method for reducing the turn-off losses at high load currents in a practical application (cf. figure 2.5).

6.2 Additional freewheeling diode

The transformer T_{FF} of the IFF method adds a significant inductance between the gate and the source. Thereby, the first resonance frequency of the gate circuit is lowered, possibly increasing oscillations. In addition, a voltage undershoot at the source potential during turn off can add a voltage to the gate due to a positive derivative of the current i_S. Both can lead to unintended switching, especially if the bias voltage is close to the threshold voltage. If no negative bias voltage is used, normally off GaN HEMTs are especially susceptible to this [133, 134]. An additional freewheeling Schottky diode D_{SK} can be added as shown in figure 6.7 to prevent this behavior.

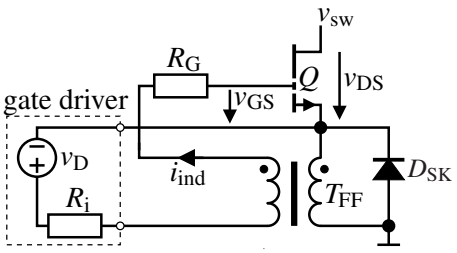


Fig. 6.7: IFF method with unipolar gate voltage and freewheeling diode for a GaN HEMT.

The figure 6.8 shows the measured turn-off transition with a GaN HEMT as Q. A bias voltage of 6 V is chosen and R_G is set to 12 Ω to damp the oscillations. However, for a current I_L = 25 A, the GaN HEMT still switches on 50 ns after the turn-off voltage transition due to a voltage undershoot at the source. By adding D_{SK} this malfunction can be prevented and the ringing from the source is not transferred to the gate anymore. However, since the threshold voltage is very low, the turn-off duration of the GaN HEMT is extended. To reduce the turn-off losses, a negative bias voltage is advantageous.

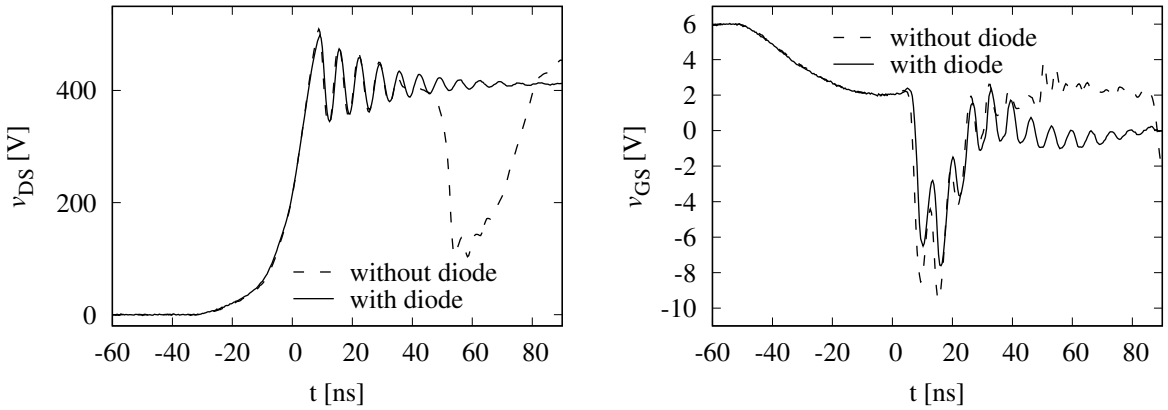


Fig. 6.8: Drain-source and gate-source voltage of a GaN HEMT during turn off with I_L = 25 A.

6.3 Robust turn on of GaN GITs

Many GaN power transistors contain a p-n junction between the gate and the channel region close to the source. In order to maintain the on-state, current must be continuously supplied to the junction, and the devices are referred to as GaN GITs (cf. chapter 2.1). This is particularly important during turn on due to the additional gate current which is necessary to charge the Miller capacitance. Otherwise, the displacement current through C_{GD} can reduce the hole injection into the electron gas channel. Thereby, the transition is delayed or even interrupted. To compensate the displacement current, the commonly recommended approach uses a high positive gate bias voltage to increase the gate current through a boost circuit. In comparison to this conventional approach, the inductive feed-forward method provides a stable turn on with a reduced bias voltage. This chapter will compare both approaches; notice that the analysis of the conventional approach already has been published previously.

6.3.1 Conventional approach and its limitations during hard switching

The figure 6.9 shows a circuit diagram of the conventional gate driving setup. Since normally off GaN HEMTs have a low threshold voltage, a negative gate bias for turn off is recommended as described in chapter 6.2. Hence, a gate driver with separate outputs for V_{Don} and V_{Doff} is utilized. Thereby, the charging of the gate through the gate resistance in series with the positive bias voltage R_{Gon} can be controlled independently of the discharging through the gate resistance in series with the negative bias voltage R_{Goff}. For the fast turn on, a higher gate current is desired, which can be provided by a boost circuit reducing the initial impedance through a boost capacitance C_{Boost} and a boost resistance R_{Boost}.

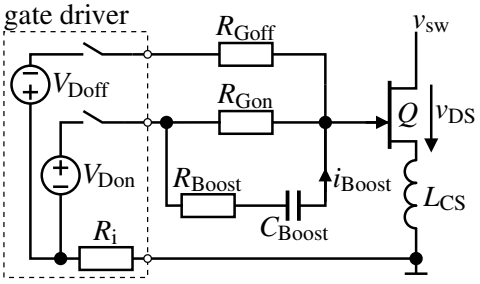
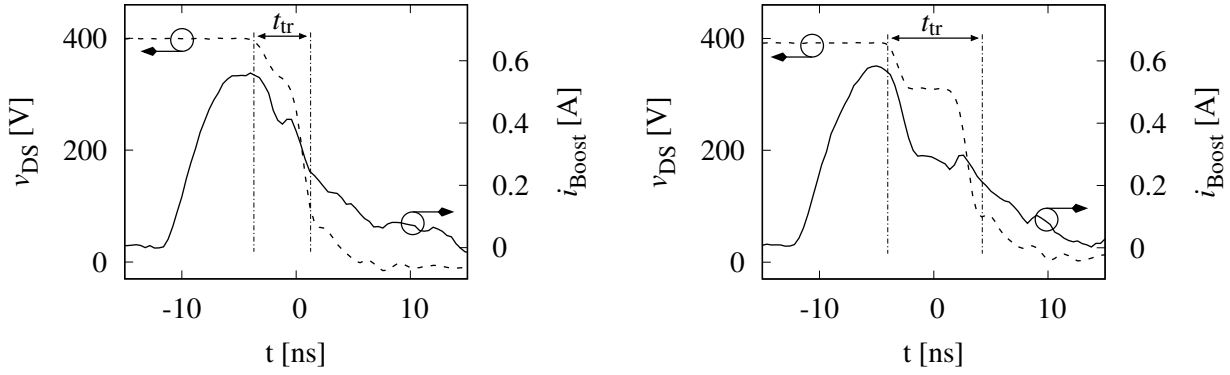


Fig. 6.9: Conventional gate driving circuit for GaN-GITs using a boost circuit.

The limiting factor of the conventional approach is the effectiveness of the additional boost current i_{Boost}. During turn on, the rising current i_{S} causes a voltage drop across L_{CS}, reducing the effective gate-source voltage. To reduce L_{CS} and thereby its impact, an additional Kelvin contact is used for the gate loop. However, the effect is still noticeable. figure 6.10(a) shows that the first voltage drop from 400 V to 310 V caused by L_{CS} has only a modest influence on the boost current for a load current of I_{L} = 5 A. For v_{DS} a slew rate of 160 V/ns was achieved between 250 V and 100 V.



(a) I_{L} = 5 A (b) I_{L} = 25 A

Fig. 6.10: Drain-source voltage v_{DS} and boost current i_{Boost} of the conventional approach.

However, for the load current I_{L} = 25 A in figure 6.10(b), the transition time t_{tr} and especially the duration up to the second voltage drop from around 310 V to 60 V increases. In addition to the reduction of i_{Boost} due to L_{CS}, the capacitance C_{Boost} is charged during the transition decreasing the voltage over R_{Boost}, further reducing i_{Boost}. Therefore, only half of the peak value of i_{Boost} is left at the end of t_{tr}. Therefore, the slew rate decreases to 120 V/ns between 250 V and 100 V. If the current I_{L}, and therefore the transition time, is increased further, charging the Miller capacitance leads to an unwanted turn off because the electron channel is not maintained anymore. The only design measure is to increase i_{Boost} until the limit defined by the maximum dynamic gate current limitation $I_{\mathrm{G,max,dyn}}$ of the device is reached. $I_{\mathrm{G,max,dyn}}$ is often ignored by different approaches that use a high boost current to increase the slew rate [135].

6.3.2 Inductive feed-forward method: Implementation and advantages

The effect duration of a boost circuit is limited as discussed in chapter 6.3.1. Furthermore, the gate current is limited to the $I_{\mathrm{G,max,dyn}}$ of the device. Therefore, hard switching of a high load current becomes critical. The inductive feed-forward method can be used to realize a stable turn on, especially for higher I_{L}. T_{FF} is introduced between the source and gate of the GaN GIT Q; see figure 6.11. In addition, a rectifier is necessary to utilize the negative swing of i_{S} which occurs

during ringing. Without the rectifier, the negative swing of i_S would reduce i_G and result in an unwanted turn off. Since the device is current controlled (e.g. equation 2.3) the impact of a reduced i_G is more significant than for the other semiconductor designs. Schottky diodes are used due to the fast reverse recovery and low forward voltage drop. The influence of T_{FF} on the turn off is minimized due to the separate discharging through R_{Goff}. The resistor R_{Gon} limits the current i_G after turn on. Since, contrary to the conventional approach, the additional gate current due to the transformer T_{FF} is independent from the gate bias voltage, V_{Don} can be reduced.

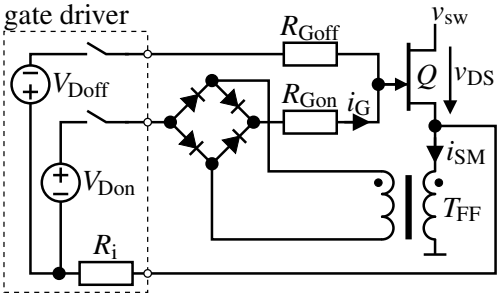
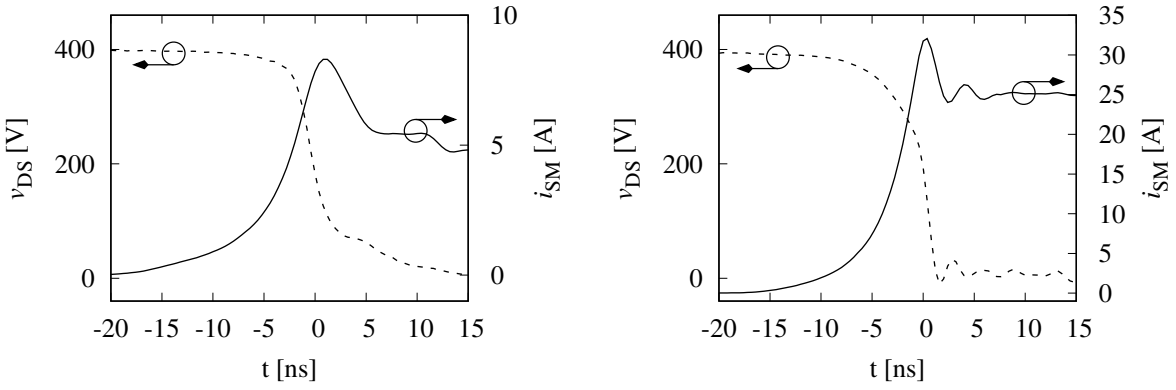


Fig. 6.11: Inductive feed-forward method with additional rectifier necessary for GaN GITs.

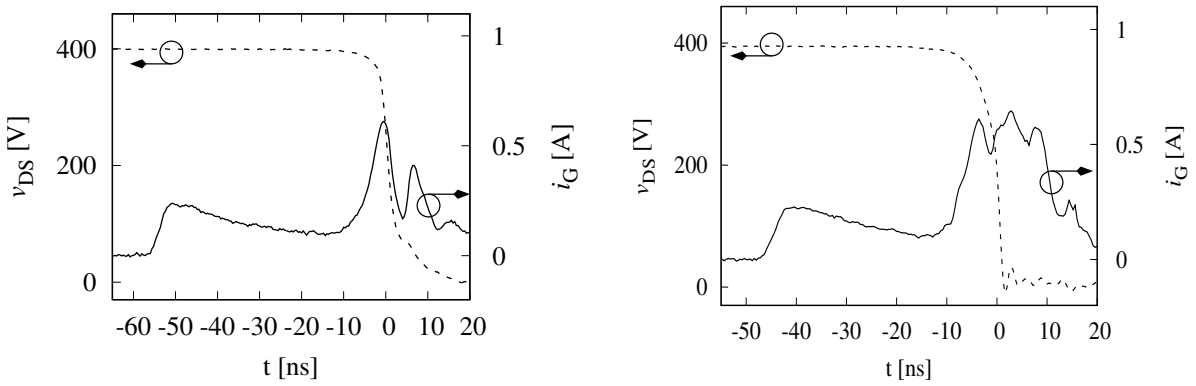
As for a MOSFET, adding the transformer T_{FF} results in a steadily increasing current gradient during turn on. However, for the GaN GIT more holes are supplied to the electron gas channel, thereby lowering its resistance and thus accelerating the transition over time. The acceleration of the turn-on transition can be seen in figure 6.12 for the I_L of 5 A and the I_L of 25 A. For 5 A the current gradient of 1.5 A/ns between 5 A and 6 A results in a maximal slew rate of 100 V/ns. Notice that the transition slows down during the current peak. Increasing I_L to 25 A significantly raises the current gradient to 40 A/ns between 20 A and 30 A, resulting in a maximal slew rate of 165 V/ns.



(a) $I_L = 5$ A (b) $I_L = 25$ A

Fig. 6.12: Switching characteristics of the GaN GIT during hard turn on with the IFF method.

Both the acceleration for increasing load current I_L and the slower transition for lower I_L can be explained by the gate current i_G shown in figure 6.13. For both load currents, i_G increases steadily once the current gradient increases noticeably around 10 ns before the maximum slew rate is achieved. However, for the I_L of 5 A, due to the lower current gradient, the discharging of the capacitance of the switching potential results in a protracted current peak; see figure 6.12(a). Therefore, i_G already significantly decreases, thereby slowing down the voltage transition. Since a significantly higher current gradient is achieved for the I_L of 25 A, the current peak duration can be shortened and thereby also the reduction of i_G is minimized.



(a) I_L = 5 A (b) I_L = 25 A

Fig. 6.13: Current i_G through R_{Gon} during the turn-on transition with the voltage v_{DS} as a reference.

To evaluate the effectiveness of the IFF method for GaN GITs, the turn-on characteristics have to be compared to the conventional approach. As previously mentioned, an important limit of these devices is the maximum dynamic gate current limitation $I_{G,max,dyn}$. To achieve similar preconditions for both approaches, the circuits are designed to achieve a comparable maximum gate current $i_{G,max}$, as can be seen in figure 6.14. Afterwards, $E_{turn\text{-}on}$ was measured from t_n = -20 ns to t_p = 15 ns as described in chapter 3.1.1.

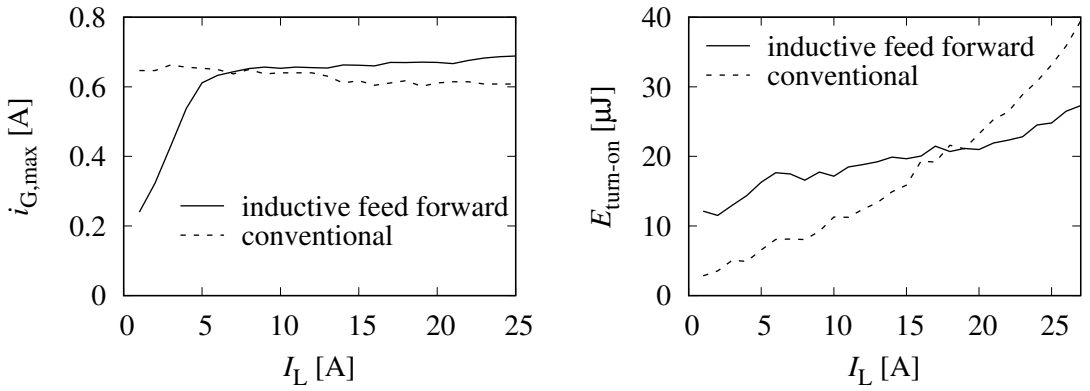


Fig. 6.14: Comparing $i_{G,max}$ and $E_{turn\text{-}on}$ of the conventional approach and the IFF method.

The turn-off losses of both approaches are comparable and almost constant in the considered load current range with around 20 µJ. Therefore, around an I_L of 17 A, the IFF method becomes more efficient. Furthermore, compared to the IFF method, other implementations that only use a V_{Don} of around 5 V report around double the $E_{turn\text{-}on}$ during hard switching [21, 136]. However, the results cannot be simply transferred to other designs. The capacitance of the switching potential in combination with the current gradient is responsible for the current peak duration and therefore the time period in which the effectiveness of the IFF method is reduced. The PCB layout and the component characteristics, therefore, have a major influence on the switching characteristics. Increasing the gate inductance could reduce the reduction of i_G during the current peak. Since thereby the effectiveness of the IFF method in the beginning of the transition is decreased, the overall $E_{turn\text{-}on}$ is increased. In general, for GaN GITs it can be stated only that the IFF method is advantageous for high load currents.

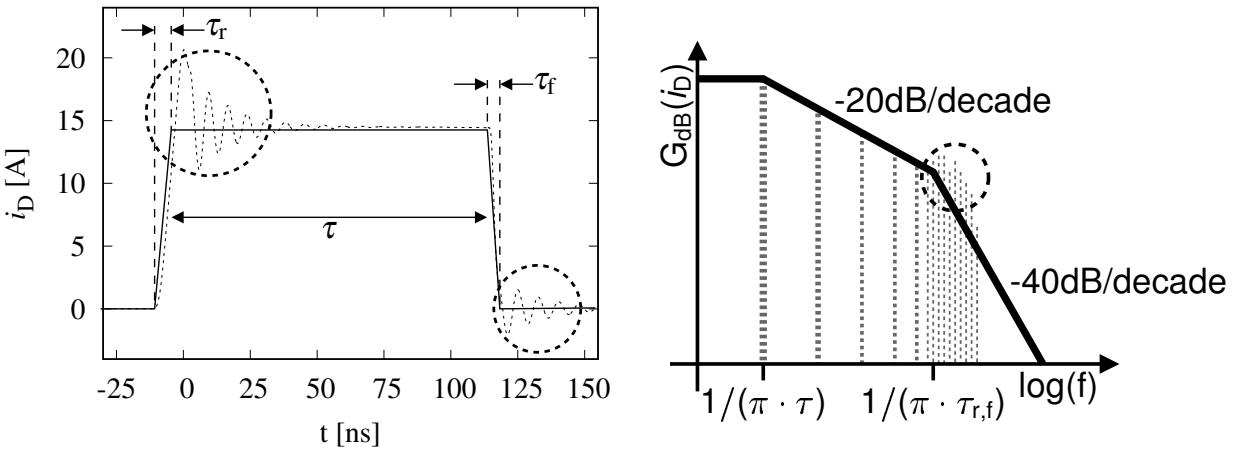
6.4 Influence of the inductive feed-forward method on the EMI

It has been shown that the IFF method decreases the transition duration and thereby the switching losses; cf. chapter 6.1. Furthermore, the current gradient and overshoot increases. Both can have significant influence on the EMI. EMI analysis is usually divided into common mode noise and differential mode noise. Fast slew rates are causing common mode noise, which results in a displacement current via attached parasitic capacitances. The differential noise is caused by the high gradient of the switching current in the commutation loop and from the reverse recovery of the diodes [26, 137]. Especially this differential noise in the form of radiated emissions is effected by the IFF method as will be shown in this chapter.

A first estimation of the influence on the EMI is possible by considering the impact of the current acceleration on the frequency domain of the signal. The output signal of a half bridge circuit is often idealized by a trapeze [138]. A corresponding signal is shown in figure 6.15 in the time domain as well as the freqency domain. For a simple transformation between the domains, it is assumed that the rise time τ_r and the fall time τ_f are equal. In that case, the amplitude density of the frequency domain can be easily obtained:

$$G_\mathrm{dB} = 20\log\left(\frac{2A\tau}{T}\right) + 20\log\left|\frac{\sin(\pi\tau f)}{\pi\tau f}\right| + 20\log\left|\frac{\sin(\pi\tau_{\mathrm{r,f}} f)}{\pi\tau_{\mathrm{r,f}} f}\right|. \tag{6.1}$$

In the equation A corresponds to the amplitude, τ to the average on-time and f to the frequency of the signal in the time domain. The amplitude density of the ideal trapeze signal is illustrated by the solid line in figure 6.15(b) which decreases with 20 dB/decade after first breakpoint at $1/(\pi \cdot \tau)$ and with 40 dB/decade after the second breakpoint at $1/(\pi \cdot \tau_{\mathrm{r,f}})$.



(a) time domain (b) frequency domain

Fig. 6.15: Ideal and actual signal with framed influence of the ringing due to fast switching.

However, in the actual current slope of i_D, depicted in figure 6.15(a) by the dotted line, ringing occurs right after the transition. The ringing is caused by the parasitic elements of the commutation loop as well as the semiconductors [139]. The deviation from the ideal trapeze results in a higher amplitude of the signal in the upper frequency domain. Especially the transition at $1/\pi\tau_{r,f}$ is affected, as highlighted in figure 6.15(b). Modern techniques to reduce the EMI use this understanding and shape the edges of a signal accordingly [29].

To measure the actual EMI of the IFF method, the double pulse setup is not sufficient since continuous operation is necessary. Therefore, a simple boost converter was realized, stepping up a supply voltage V_{sup} of 150 V to an output voltage V_{out} of 380 V with a switching frequency of 380 kHz. A basic circuit with the additional coupling networks which are necessary to measure the conducted emissions can be seen in figure 6.16. Neither the gate driver nor the additional controller and its circuitry are shown. Detailed information to the circuit can again be found in the appendix. Since EMI measurement setups and limits are changing with the applied standards, the IFF method was again compared with a conventional gate driver; cf. figure 3.4. This allows to make a relative statement about the influence of the IFF method.

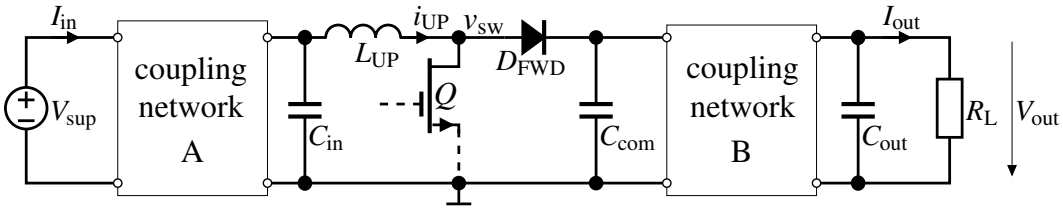
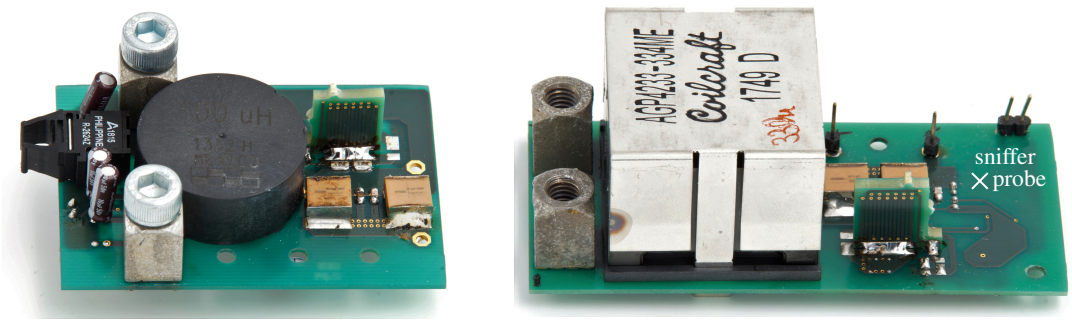


Fig. 6.16: Boost converter with additional coupling networks to measure the EMI.

To demonstrate the influence of the current ripple on the IFF method, two different setups are realized; see figure 6.17. For a constant switching frequency, the current ripple can be controlled by the main inductor of the boost converter L_{UP} since the duty cycle is fixed for the chosen voltage relation. One inductor with 100 µH and another with 330 µH were chosen for the two setups.



(a) L_{UP} = 100 µH (b) L_{UP} = 330 µH

Fig. 6.17: Analyzed boost converter with applied IFF method, easily distinguishable by L_{UP}

The commutation loop as well as the gate driver connections are similar to make both setups comparable. The efficiency of both setups was measured to asses the performance. For this, the output current I_{out} was increased from 0.2 A up to around 1.32 A in 10 mA steps. At every step the input current I_{in} and I_{out} are measured with an additional shunt and V_{sup} as well as V_{out} are determined close to the converter with the coupling networks removed. A comparison of both setups which also includes the conventional approach (by removing the transformer T_{FF}) can be seen in figure 6.18. The efficiency of the IFF method increases towards the conventional approach. The gain is higher for the 330 µH setup compared with the 100 µH setup, especially for a higher output power $P_{out} = I_{out} \cdot V_{out}$. This is due to the lower current ripple of the 330 µH setup. By reducing the current ripple, in continuous operating mode the discrete semiconductor Q is turned on during a higher current for the same P_{out}. A higher current during turn on increases the losses in the semiconductor but also increases the gain due to the IFF method (e.g. figure 3.9). The same effect can be achieved by increasing the frequency [25].

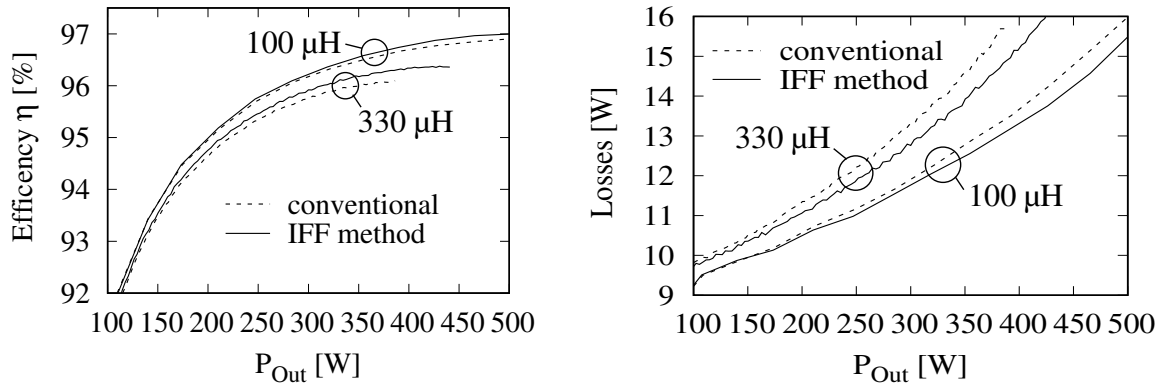


Fig. 6.18: Efficiency and losses of the different boost converter setups.

Furthermore, this effect can be seen more clearly by the losses in figure 6.18. In addition, the transition from discontinuous to continuous operating mode has recognizable effects. For the 330 µH setup this transition occurs around P_{out} = 150 W and for the 100 µH setup at around P_{out} = 400 W. For both setups, the losses increase significantly for a P_{out} above this threshold due to the higher current during turn on of the semiconductor. Especially for the 100 µH setup it is recognizable, that even in discontinuous mode with a P_{out} below 400 W the IFF method nevertheless reduces the losses. At this operating point, the additional inductance in the gate loop has a significant influence on that gain. Due to the high switching frequency compared with the low voltage relation and output current, the switching losses of the semiconductor have a major impact on the overall losses. At a P_{out} of around 16 W the semiconductor losses started to be to high, which results in its destruction. Due to the higher efficiency, the IFF method can therefore be used for a higher output power range than the conventional approach.

To compare the EMI of the IFF method to the conventional approach, a operation point with a significant efficiency difference was chosen. This requires that the boost converter is run in continuous operation mode and turns on during a high current, which is implying a low ripple. The characteristics of the switching potential are shown in figure 6.19 for the 330 µH setup and an I_{out} of 1 A. The semiconductor is turned on at around 1.4 µs while the boost converter inductor current i_{UP} is around 0.6 A, which is close to the destruction of the MOSFET and therefore offers almost the highest possible efficiency gain. For this operating point the efficiency is increased from 96 % to 96.3 %. This corresponds to a loss reduction of around 1 W. For the 100 µH setup the efficiency only increased from 96.6 % to 96.7 % reducing the losses by 0.35 W. The overall higher efficiency results from half the winding resistance as well as the reduced remagnetization losses of the 100 µH inductor.

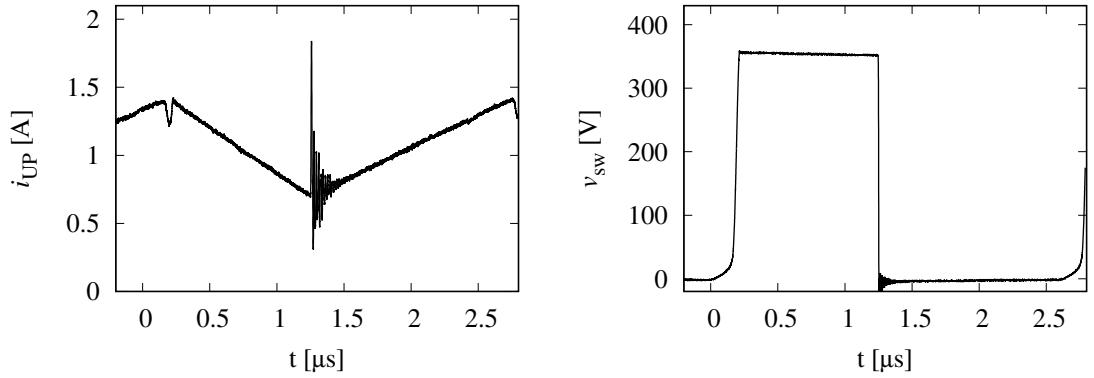
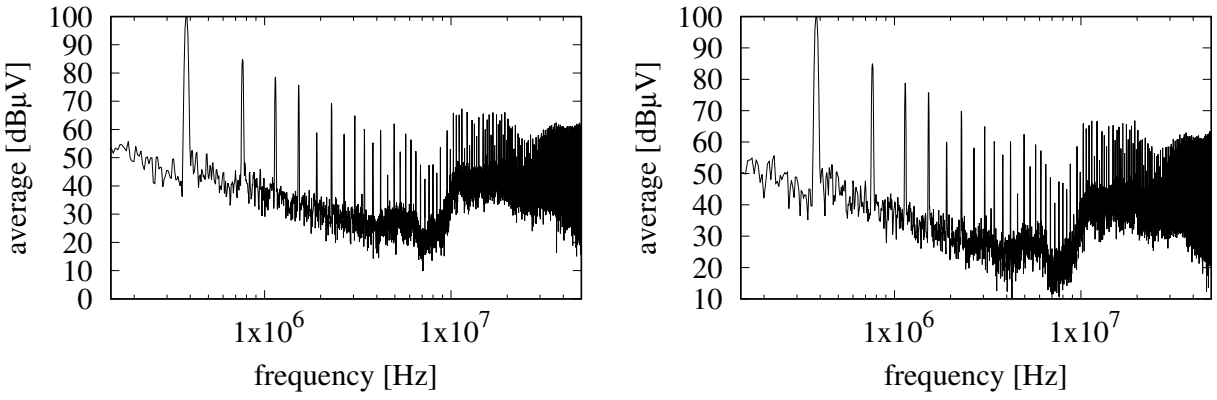


Fig. 6.19: Continuous operation mode of the 330 µH setup for an I_{out} of 1 A.

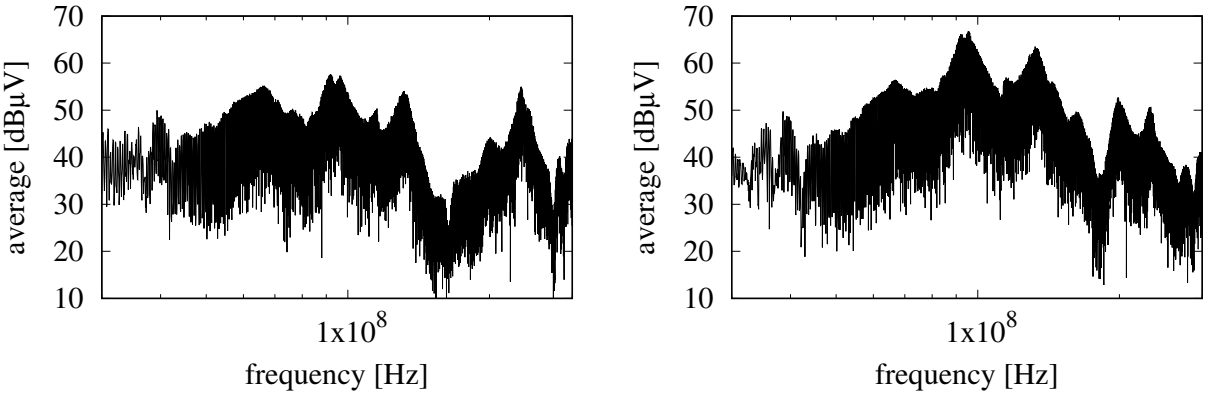
The conducted emissions are measured at the input and the output of the converter. Since L_{UP} is creating a low pass filter in combination with the input smoothing capacitor (C_{in}) of the boost converter, the measurement at the output is expected to show the majority of the possible effects of the IFF method. To connect the EMI receiver a line impedance stabilization network for automotive applications is used as a coupling network [140]. The cabeling was fixed so that its position is not changing between the tests. The detector of the EMI receiver is set to average mode and a resolution bandwidth of 9 kHz. For the conducted emissions the common measurement range starts at 150 kHz and goes up to 30 MHz. In figure 6.20 the measurement results at the output are presented for a slightly wider range (100 kHz - 50 MHz) at the coupling network B. There is no difference between the conventional approach and the IFF method. The switching frequency of around 380 kHz is clearly visible with the highest peak of 100 dBµV. The measurements at the coupling network A have shown an overall reduction of this peak. In addition, the peak of the conventional approach was further reduced (ca. -0.5 dBµV). This is probably due to the higher efficiency and therefore lower I_{in}. Overall the influence of the IFF method on the conducted emissions is insignificant for the considered semiconductor.



(a) conventional (b) IFF method

Fig. 6.20: Measurement of the conducted emissions at the coupling network B.

Another important aspect of the EMI are the radiated emissions. To get an impression on the impact of the IFF method on these emissions, a sniffer probe was placed next to the commutation loop. The round probe with an inner diameter of 3 cm was placed 2 cm above the position marked in figure 6.17(b). A casing of mu-metal was added to prevent interference of the ambient environment with the measurement. To realize the same commutation loop, and therefore the same distance to the sniffer probe, this time the conventional approach was realized with the additional transformer T_{FF} but the output of the secondary winding was left open. The measurement range was set from 26 MHz up to 300 MHz and a resolution bandwidth of 120 kHz is chosen. The results in figure 6.21 show that the radiated emissions are increasing significantly for the IFF method around 90 MHz. This is correlating with the bandwidth of the current gradient as analysed in the beginning of this section and is also caused by the higher peak current of the IFF method, cf. figure 3.6. The impact of the IFF method on the radiated emissions is thus significant and has to be taken into account. For applications with lower transients such as energy and signal transfer to the gate driver, the thus lower radiated emissions of coreless transformers can be uncritical [141].



(a) conventional (b) IFF method

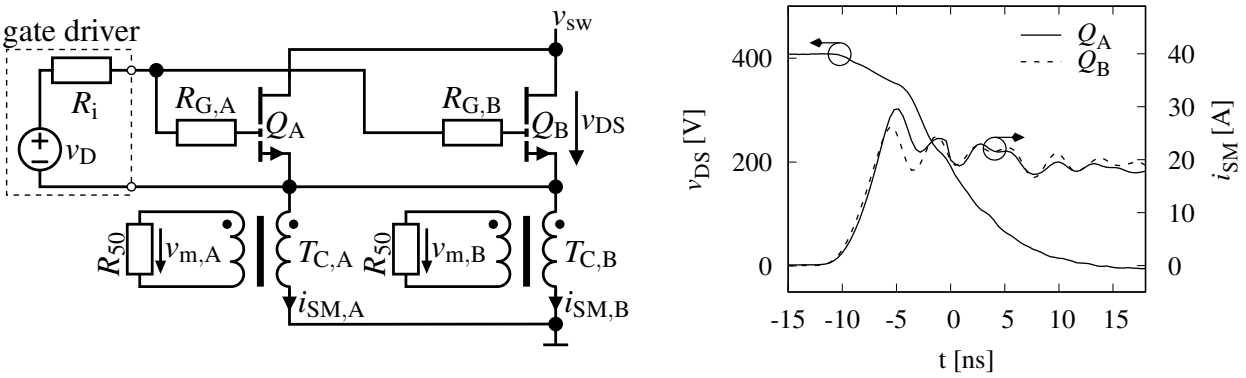
Fig. 6.21: Measurement of the radiated emissions with a sniffer probe.

6.5 Applying the IFF method to parallel connected power semiconductors

For high current ratings, power modules operate several semiconductors in parallel. Thereby, smaller devices can be used, increasing the yield and reducing the system cost. In addition, the losses can be distributed, reducing the thermal impedance. Power semiconductor normally have a positive temperature coefficient: with an increase in junction temperature, the on-state resistance also increases. Thus, only an effective thermal coupling is necessary for current balancing in steady state. The challenge is now to ensure that the transition losses are also equally distributed. Fast switching transitions increase the influence of stray inductance and the drain-gate capacitance and thereby amplify current imbalances [142]. Improvements can be achieved by focusing on the design of the PCB, see [143]. Especially the common source inductance has to be minimized and a higher inductance of the connection between the switching potential and the drain of the single semiconductors can reduce current imbalances [144]. Device tolerances limit this approach, since the resulting unbalances in the switching losses can cause thermal runaway at high frequency operation [145]. Especially differences of the threshold voltage and the transconductance can have a significant influence on current imbalances [146].

A resistor in the series with the semiconductor is a simple approach to balance the currents in parallel semiconductors [147]. Since this is resulting in additional losses during turn on, this approach is not favorable for high current applications. A more appropriate procedure for high current applications is to create a voltage drop over an inductance. If additional resistors are placed between source and the gate driver reference connection, the resulting voltage difference in the source of the paralleled semiconductors can be used to balance the currents. The voltage drop over the additional resistor slows down the faster semiconductor and accelerates the slower semiconductor [148]. Another approach to force a balancing of the current is to use the windings of a transformer each added in series to the drain connections of two paralleled power semiconductors [149]. However, both approaches can increase the inductance of the commutation loop significantly and thereby increase the over-voltage peak during turn off. The current imbalance can also be reduced by adjusting the dead time of the gate driver if for each gate a separate one is used [150]. For this approach the imbalance has to be measured or known beforehand and a lot of additional circuitry is necessary. Anyway, it shows that also the inductance in the gate can affect the current imbalance.

This chapter focuses on the homogeneous distribution of turn-on switching losses by applying the IFF method. Since the turn-on losses in hard-switching applications are usually at least three to four times higher than the turn-off losses (cf. figure 3.9(a), as well as comparing figure 6.4 and figure 6.6), this can significant help balancing the losses of parallel connected semiconductors. To get a reference of the current distribution during fast transients, GaN-HEMTs are used. In figure 6.22(a) two semiconductors are connected in parallel and a single gate driver is attached with two conventional gate resistors in series to the gates. To achieve a low additional stray inductance, and achieve a wide bandwidth, an inductive measuring method was used. However, instead of the current sensor from chapter 5, the voltage across the secondary winding of a coreless transformer T_C was directly measured over a 50 Ω resistor and the current shape is reconstructed digitally [123].



(a) equivalent circuit (b) switching characteristics

Fig. 6.22: Conventional setup with two parallel GaN-HEMTs as well as the i_{SM} measuring method. The corresponding switching characteristics show the current imbalance during turn on.

Since the layout was designed compact to achieve a minimal difference in stray inductance, cross coupling between both transformers $T_{C,A}$ and $T_{C,B}$ can be critical. The measured induced voltage (v_m) of both semiconductors Q_A and Q_B can be described by:

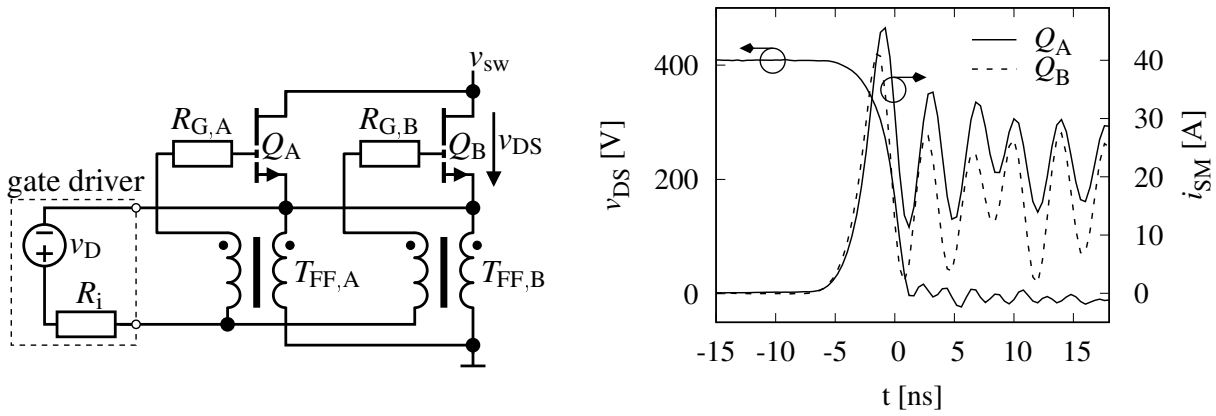
$$v_{m,A} \approx M_A \cdot \frac{di_{SM,A}}{dt} + M_{AB} \cdot \frac{di_{SM,B}}{dt} + v_{offset}. \tag{6.2}$$

$$v_{m,B} \approx M_{BA} \cdot \frac{di_{SM,A}}{dt} + M_B \cdot \frac{di_{SM,B}}{dt} + v_{offset}. \tag{6.3}$$

M represents the mutual inductance between the transformer windings. The primary winding of T_C is connected in series to the source and the secondary winding parallel to the 50 Ω resistor. For $T_{C,A}$, the desired output signal at the secondary winding related to the $di_{SM,A}$ at the primary winding is created by M_A. M_{AB} is the mutual inductance between the secondary winding of $T_{C,A}$ and the primary winding of $T_{C,B}$ which introduce an unintended influence of $di_{SM,B}$. To obtain the exact current, the mutual inductance has to be considered during the digital reconstruction.

Therefore, through a calibration measurement, separately switching a defined current through both measurement lines, the mutual inductance was extracted. For the test setup, M_A and M_B are around 1 nH, M_{AB} and M_{BA} around 10 pH. Afterwards, with both signals $v_{m,A}$ and $v_{m,B}$ the actual current can be calculated, using equation 6.2 and 6.3. The unavoidable offset voltage v_{offset} can be ignored since its eliminated during the integration necessary to determine i_{SM}. Since the induced current is significant lower than i_{SM}, its influence and therefore the mutual inductance between the secondary windings of $T_{C,A}$ and $T_{C,B}$ was neglected. In figure 6.22(b) the resulting switching characteristics for a double pulse measurement with a supply voltage of V_{sup} = 400 V and an I_L of 40 A are shown. The current I_L splits into both conducting paths and is measured as $i_{SM,A}$ and $i_{SM,B}$. Because of production tolerances, the GaN-HEMTs do not have the same threshold voltage. In addition, the layout is slightly asymmetrical, resulting in different gate impedances. Therefore, the current in Q_A increases faster and the switch is carrying a higher current than Q_B through the transition. This results in different switching losses for both semiconductors.

The IFF method is now applied in two different ways to the parallel connected power semiconductors. First, in figure 6.23(a) the IFF method was used on both lines separately. The primary winding of T_{FF} is connected in series to the source and the secondary winding in series to the gate of the same semiconductor. Again, the IFF method results in a raise of the current gradient during the turn-on transition and thereby also amplifies the current overshoot and ringing. The current in figure 6.23(b) still shows a current imbalance which is comparable to the conventional approach. Note that the slew rate is increased to 110 V/ns between 330 and 50V. For the same voltage difference the conventional setup only achieves a slew rate of 30 V/ns.

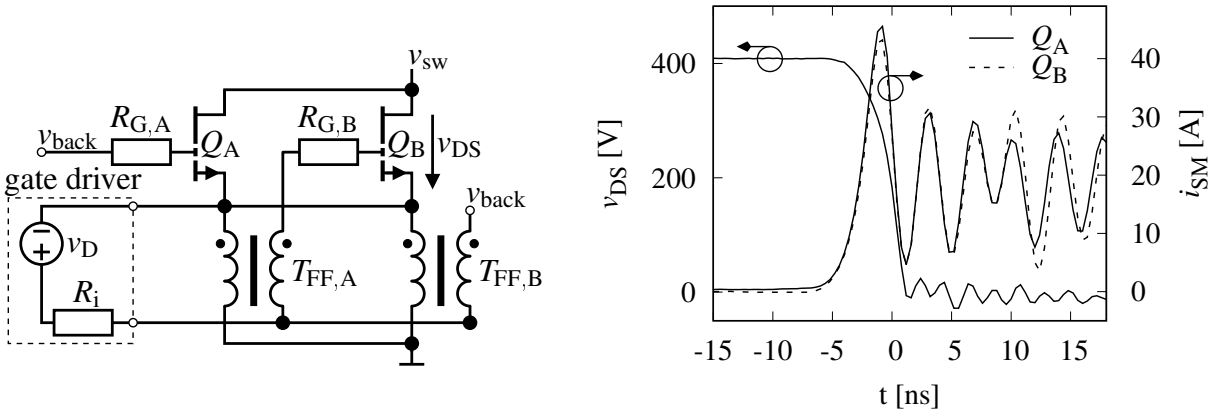


(a) equivalent circuit

(b) switching characteristics

Fig. 6.23: Parallel applied IFF method on two parallel GaN-HEMTs with corresponding switching characteristics still showing a current imbalance during turn on.

Secondly, in figure 6.24 the IFF method was used to cross couple the semiconductors. The primary winding of T_{FF} is connected in series to the source of one semiconductor and the secondary winding in series to the gate of the other semiconductor. Again, only a single gate driver was used. Instead of switching independent, the faster semiconductor accelerates the turn on of the slower semiconductor through the IFF method. The adjacent switching characteristics show that the currents in both semiconductors are almost identical. A comparable slew rate as for the parallel applied IFF method was achieved.



(a) equivalent circuit (b) switching characteristics

Fig. 6.24: Cross-coupled IFF method on two parallel GaN-HEMTs with corresponding switching characteristics showing a balanced current during turn on.

The measurements have been repeated with a higher gate resistor. Thereby, the transition times for all approaches decreased, resulting in a lower slew rate. A uniform distribution of the turn-on losses can still be achieved for the cross-coupled version. However, especially the conventional setup shows an increase in the current imbalance.

To determine how the turn-on losses depend on the inductive load, the switched current I_L is increased from 10 A to 45 A in 1 A steps. For every step, the turn-on losses are determined for the period where $i_{SM} \geq 0.1 \cdot I_L/n$ where n is the number of parallel HEMTs and $v_{DS} \geq 0.1 \cdot V_{sup}$. This is contrary to the approach in chapter 3.1.1, but offers a sufficient accuracy for the switching losses of GaN-HEMTs.

The results are shown in figure 6.25 for both implementations of the IFF method and in each case compared to the conventional approach. In the conventional setup, one of the semiconductors always has higher losses than the other, even though it was ensured in the design of the PCB that the GaN-HEMTs are as close to each other as possible and have a comparable inductance in series. For higher I_L the current imbalance increases which can be seen in the spread of the turn-on losses. For the parallel IFF method, the current imbalance remains but stays constant even for

increasing load currents. This can be identified by the constant offset between the turn-on losses in both semiconductor. The cross-coupled approach shows a uniform distribution of the turn-on losses. Both implementations of the IFF method reduce the turn-on losses by 50 % for the highest I_L compared to the conventional setup due to the faster transition.

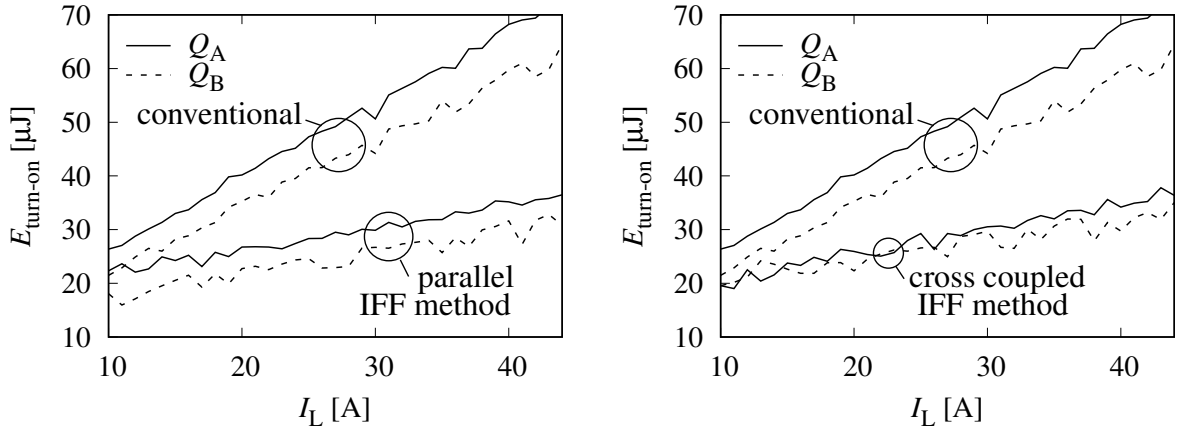


Fig. 6.25: Comparing the turn-on losses of the different IFF methods to the conventional approach.

The cross-coupled approach promises advantages for multiple semiconductors connected in parallel. A chain of multiple semiconductors can be set up to always accelerate the next semiconductor until the transformer T_{FF} of the last semiconductor connects back to the first one. The limiting factor is the impedance of the gate loop and the delay on the IFF method created by it. The current overshoot could be reduced by slower transitions. Further improvements could also be achieved by using the novel design of a coreless planar transformer from chapter 4.2. For the results in this chapter, the design in chapter 4.2.2 was used. Primary and secondary winding were isolated by Kapton tape with a thickness of 50 µm and a permittivity of $\varepsilon_r = 3.6$ [111]. The distance I of the transformer windings results in a very high capacitance C_K (cf. chapter 4.2.2). In figure 6.26 the v_{GS} of a single GaN-HEMT with a comparable gate loop and the transformer T_{FF} used in this chapter is shown.

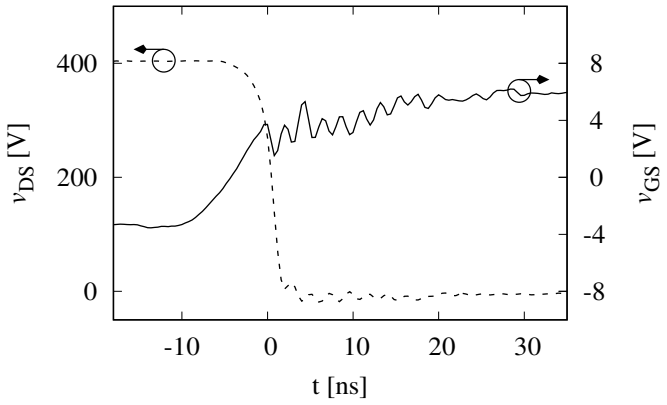


Fig. 6.26: Influence of the IFF method on the v_{GS} of a single GaN-HEMT for $I_L = 8$ A.

In contrast to the v_{GS} slope of the SJMOSFET in figure 6.2, for the GaN-HEMT no significant voltage peak before the voltage transition of v_{DS} at $t = 0\,s$ is visible. This temporary boost of the gate driver voltage was throughout this work declared as the beneficial characteristic of the IFF method. During the acceleration of the GaN-HEMT, the additional voltage of T_{FF} is compensated by the voltage drop of the package inductance L_{CS} (cf. figure 2.1) due to the higher current gradient of the device. This inductance has to be considered since for this package there is no Kelvin connection. Therefore, even a higher acceleration of the turn-on transition could be possible if the mutual inductance as well as the coupling coefficient of T_{FF} is improved. However, the main benefit of using the novel design of a coreless planar transformer would be the significantly lower C_K which would increase the resonance frequency of the gate loop and thereby also increase the damping due to the higher resistance of the secondary winding at high frequencies (cf. figure 4.22). This also prevents undamped oscillations which could be created due to the additional transconductance of the discrete semiconductor Q. Furthermore, in the parallel connection described in this chapter, the gate loop can not be described as simply as in chapter 3.3.5. Additional parallel pathways which have resonance frequencies of their own are added and have to be taken into account. Especially, du to the high slew rate and the resulting current over C_{GD}, most of these oscillations would be stimulated. Therefore, high damping is beneficial to prevent critical superimpositions which could lead to an unwanted turn off.

Overall, the fast transitions of GaN-HEMTs make it difficult to point out the benefits of the IFF method on parallel connected semiconductors, even though it was achieved in this chapter. By using SJMOSFETs, equipment with a lower bandwidth could be used for the measurements and the current imbalances would have a bigger impact on the switching losses due to the slower transitions. Furthermore, by using the novel design of a coreless planar transformer, the accelerating effect of the IFF method is underlined by the temporary boost of the gate driver voltage.

6.6 Applying the IFF method to SI IGBTs

Up to now, the focus of this thesis was on unipolar semiconductors since they offer fast switching transitions. Because of the low gate charge and the high current gradients, a coreless transformer was sufficient to accelerate the turn-on transition using the IFF method. IGBTs, on the other hand, are bipolar semiconductors that offer a low forward voltage but require additional time during turn on and off due to the slower minority carriers that also participate in the current flow. Instead of the linear R_{DSon} a MOSFET provides, the on-state voltage drop of an IGBT typically increases with the log of the current. However, the initial voltage drop at low load currents of an IGBT is often only feasible in high voltage applications. These are just some of the fundamental differences in the operating principles of an IGBT compared to the considered unipolar semiconductors. Therefore the basic equivalent circuit in chapter 2 does not apply to the IGBT and these are also the reasons for not consider it in the comparisons of chapter 2.1.1.

This chapter is also an exception to this work for another reason: Because of the slow switching transitions of an IGBT, the current gradients and thereby the voltage drop over an coreless inductor is reduced. Therefore, to realize the same output voltage v_{ind} of the transformer, either the turns ratio or the coupling coefficient of the transformer have to be increased, if the primary inductance should be kept small. In a coreless transformer, the turns ratio can be limited by the design, which is the case in chapter 4.2, or it can also reduce the coupling coefficient once a critical number of turns is achieved. This restrictions can be bypassed with a magnetic core which channels the magnetic field and thus achieves a high coupling coefficient, even for a high turn ratio. A flat ribbon cable core with the measures 33.5 x 12 x 6.5 mm was used to realize the transformer T_{FF} of the IFF method. The transformer as well as the final setup with the IGBT module can be seen in figure 6.27. To prevent saturation of the magnetic core due to high load currents, one side of the core was removed to create an air gap.

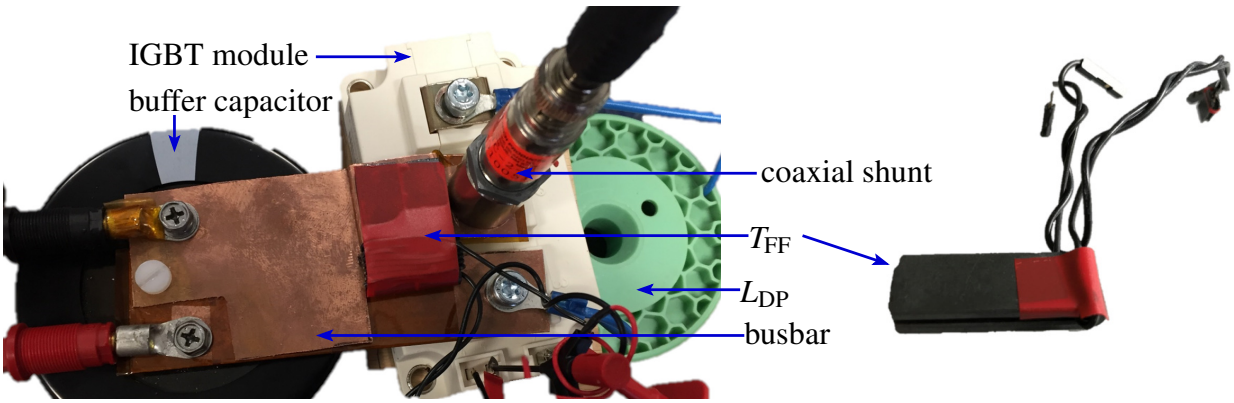
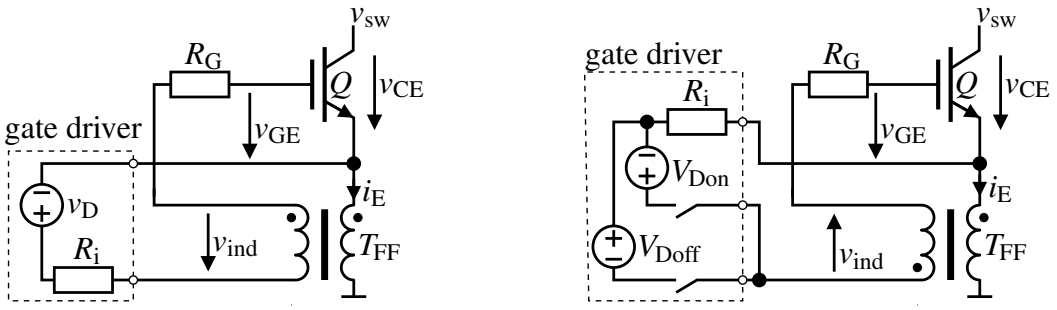


Fig. 6.27: Setup of the IGBT module, realizing the IFF method with a flat ribbon cable core.

This also allowed to easily push the core over a loop in the busbar, which is used as a primary winding for the transformer. The secondary winding only consists of a single turn, by which the IFF method was added to a conventional 1200 V IGBT half bridge module for industrial applications. Again, a double pulse setup was used to characterize the switching transitions. However, this time the lowside of the IGBT module was used as the DUT Q and the highside is a replacement for D_{FWD}. The transformer was connected in two different polarities: First, in figure 6.28(a), the IFF method was used to increase the gate voltage during turn on. Also, the polarity of the transformers secondary winding was inverted, as shown in figure 6.28(b), to temporarily reduce the gate voltage during turn on. This approach is accordingly called NIFF method.



(a) inductive feed forward (b) negative inductive feed forward

Fig. 6.28: Comparison of the gate driving methods applied to the IGBT setup.

In order to highlight the differences of the new approach, both methods are compared to a conventional setup, using only a resistor in series to the gate. The emitter current i_{E} was measured with a coaxial shunt providing a bandwidth of 400 MHz. In figure 6.29 the already extensively described influence of the IFF method on the switched current i_{E} and thus on the collector-emitter voltage v_{CE} is shown. This demonstrates, that by increasing the coupling coefficient by using a magnetic core, also for slower current gradients as shown in this example with an IGBT, the IFF method can be used to accelerate the turn-on transition.

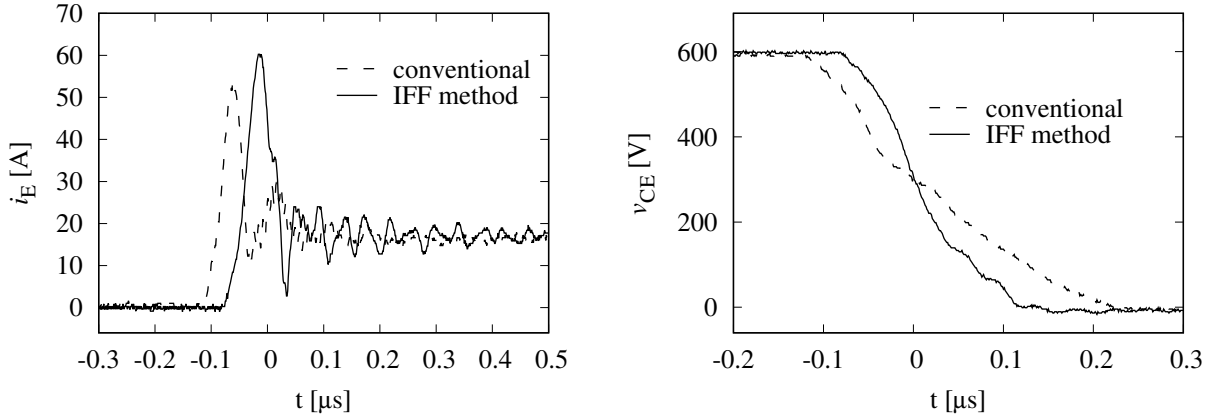


Fig. 6.29: Comparison of v_{CE} and i_{E} at turn on to show the influence of the IFF method.

Another possibility is the NIFF method, in which by changing the polarity of the secondary winding, the gate voltage is reduced during turn on. In figure 6.30 the influence on the turn-on characteristics can be seen. Instead of accelerating the turn-on transition, it is delayed. Especially, the gradient of i_E is decreased and thus also the peak current. Thereby, at first the initial voltage drop of v_{CE} due to the parasitic inductances is reduced. This can be seen between -0.3 µs and -0.2 µs, compare figure 3.2 which can also be used for an IGBT in hard-switching applications. Afterwards, also the voltage transition is extended significantly.

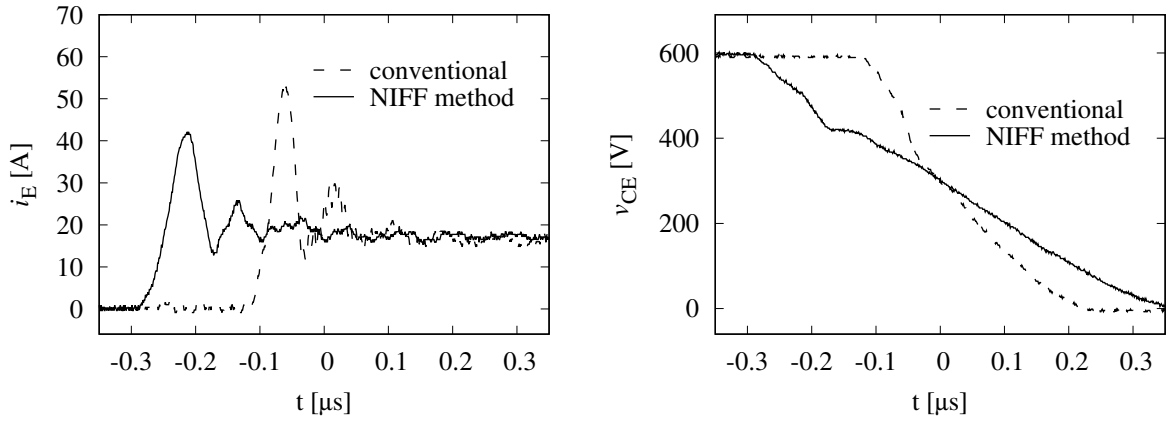


Fig. 6.30: Comparison of v_{CE} and i_E at turn on to show the influence of the NIFF method.

Up to now, the focus this work was to reduce the switching losses. With the NIFF method now these losses are increased intentionally. The advantage is the lower EMI, which is correlating to the current gradient, as is described in the beginning of chapter 6.4. Since the EMI is critical in a lot of application, typically the gate resistor is increased to slow down the transition. However, this also creates additional losses due to the higher resistance. With increasing switching frequencies, these losses can become significant. By using the NIFF method, the gate resistor can be reduced and still a slow current gradient is achieved. Furthermore, the same on-state resistance can be achieved, because once I_L is stabilized, the full gate driver voltage is transfered to the gate.

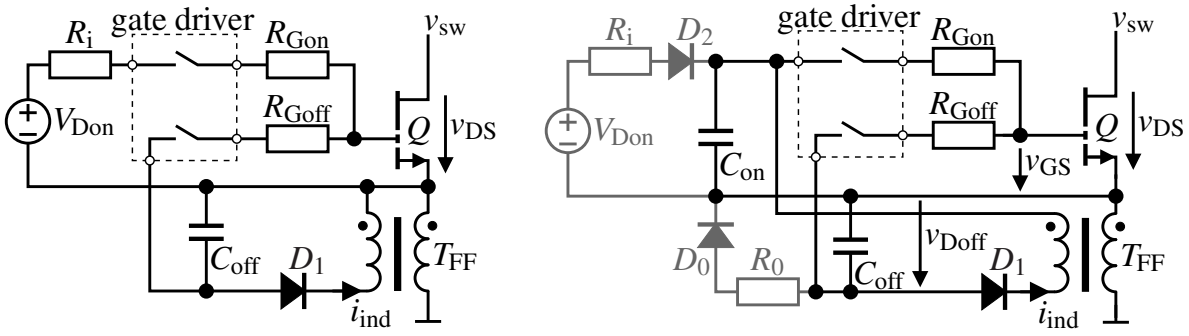
A drawback of the NIFF method is that a negative bias voltage becomes necessary. During turn off an additional voltage is applied to the gate by T_{FF} which can result in an unintended turn on. In the measurement, a V_{Doff} of around -12 V was used and therefore v_{ind} was not critical during turn off. Since V_{Don} is predefined by the required on-state resistance and v_{ind} is chosen to establish the desired turn-on transition, V_{Doff} can be used to adjust the duration of the turn-off transition.

As already mentioned earlier, the use of an IGBT is an exception in this work. The NIFF method would be more reasonable for unipolar semiconductors which are actually used in fast switching applications. Especially if the gate charge is high, the losses over an otherwise required gate resistor can be significant and can be avoided with this method.

7 Creating a negative bias voltage for gate driver

A common concept of this work are faster transitions to reduce the switching losses. In chapter 6.4 it was already stated that higher radiated emissions are a downside for hard-switching applications. Furthermore, faster transitions can also disrupt the turn off since the slew rate creates a displacement current through C_{GD} which can charge C_{GS}. High slew rates during turn off can therefore result in an unintended turn on of the semiconductor which is known as a miller-induced turn on [151, 152]. Compared to silicon devices, normally off wide bandgap semiconductor feature a low threshold voltage, and are thus susceptible to this effect. To counter this effect, reducing the impedance of the gate loop or increasing C_{GS} to reduce the peak voltage can be acceptable. However, both measures can have significant impact on the EMI or the overall switching losses. For this reason, an additional negative bias voltage (V_{Doff}) is often recommended [153]. Charge pumps can be used to generate V_{Doff}, but they add complexity. For high-side switches a buck-boost bootstrap circuit is also possible [154]. A negative gate voltage can also be generated by means of a decoupling capacitance [21]. In some applications the negative gate voltage undershoot due to ringing can be also sufficient [155, p. 46-47]. In this chapter a novel circuit will be introduced and analyzed which takes advantage of the coreless transformer of chapter 4 to realize V_{Doff}.

In chapter 3.2 the benefits of a transformer added to the source of a power semiconductor are shown for hard switching. During turn on the current gradient of i_S results in a voltage drop over the primary winding of T_{FF}. This voltage is transformed to the secondary winding and can be quite significant; cf. figure 3.7. In figure 7.1 this effect is used to create a negative voltage for V_{Doff}.



(a) discharging to the source contact (b) discharging to the positive gate driver supply

Fig. 7.1: Creating a negative bias voltage V_{Doff} by amplifying the voltage drop over an additional source inductance during turn on of the semiconductor with T_{FF}.

If the voltage over the secondary winding is high enough, the induced current i_{ind} charges C_{off}. In figure 7.1(a) the voltage drop over the secondary winding of T_{FF} has only to surpass the forward voltage of D_1 and C_{off} is thereby discharged to the source contact. In figure 7.1(b) C_{off} is discharged to C_{on} instead. The charge from C_{off} is thus reused to charge the gate of the power semiconductor. However, the voltage at the secondary winding of T_{FF} must first surpass V_{Don} added to the forward voltage of D_1 before C_{off} is discharged. For the initial start up an additional voltage source V_{Don} decoupled by D_2 as well as R_0 and D_0 to provide an initial voltage to C_{off} are necessary. In both designs the maximum negative voltage is limited by the voltage drop over the secondary winding. This voltage is based on the turns ratio and the maximum current gradient of i_S which creates a voltage drop over the primary winding.

To point out the advantages and disadvantages of the concept, a circuit following figure 7.1(b) was analyzed. Again the double pulse setup was used, see figure 3.1. Since more than two pulses are necessary to show the full transient response of the circuit, a resistor is put in series with L_{DP} to create a ripple of around 1 A with a duty cycle of 0.7 for a switching frequency f_{sw} of 150 kHz and a load current of 15 A. Thereby, the continuous operation mode of a step-up converter as in chapter 6.4 is emulated. The resulting current in the inductor L_{DP} as well as v_{DS} can be seen in figure 7.2. The voltage v_{DS} shows a high overvoltage peak during turn off due to the high slew rate of the GaN HFET for an I_L of 15 A. As can be seen in the beginning of the transition, the overvoltage peak increases from 335 V to 360 V. This is due to an increase of the slew rate from 25 V/ns to 40 V/ns caused by the decrease of the gate voltage during turn off.

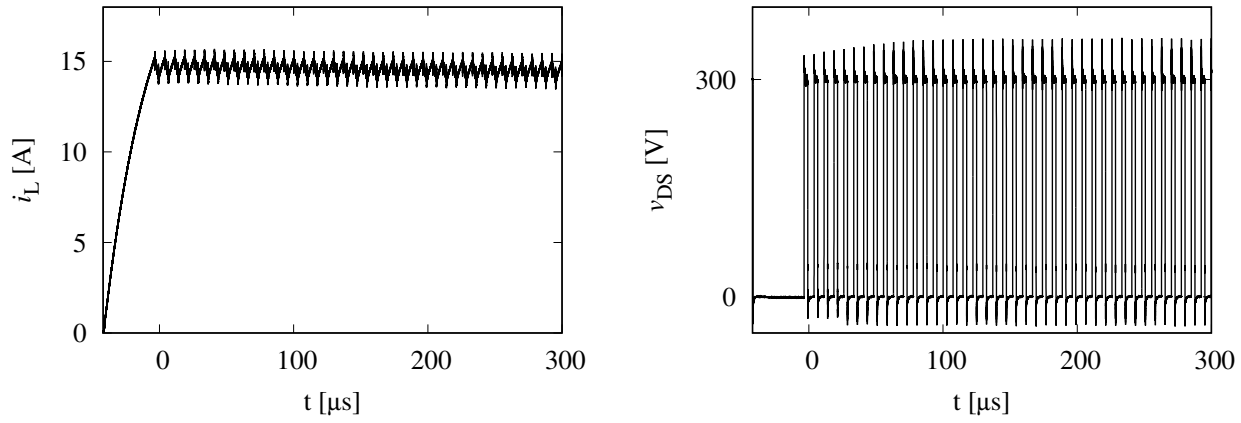


Fig. 7.2: Load current as well as the drain source voltage of the adjusted double pulse setup.

The corresponding square wave voltage v_{GS} is depicted in figure 7.3 and changes between the voltage at C_{on} during on state and C_{off} during off state. In the beginning, the voltage at C_{off} is slightly above 0 V due to the forward voltage of D_0 which sets the initial voltage at C_{off}. Afterwards C_{off} is charged with a voltage curve which shows a PT1 behavior. After a settling time of around 250 ms the final voltage of almost -2.5 V is achieved. This is clearly visible in the more detailed accompanying magnification in figure 7.3. Furthermore, the voltage at C_{on} increases slightly up to around 5.2 V over time. 5 V is the initial voltage of C_{on} which is applied by the voltage source V_{Don}.

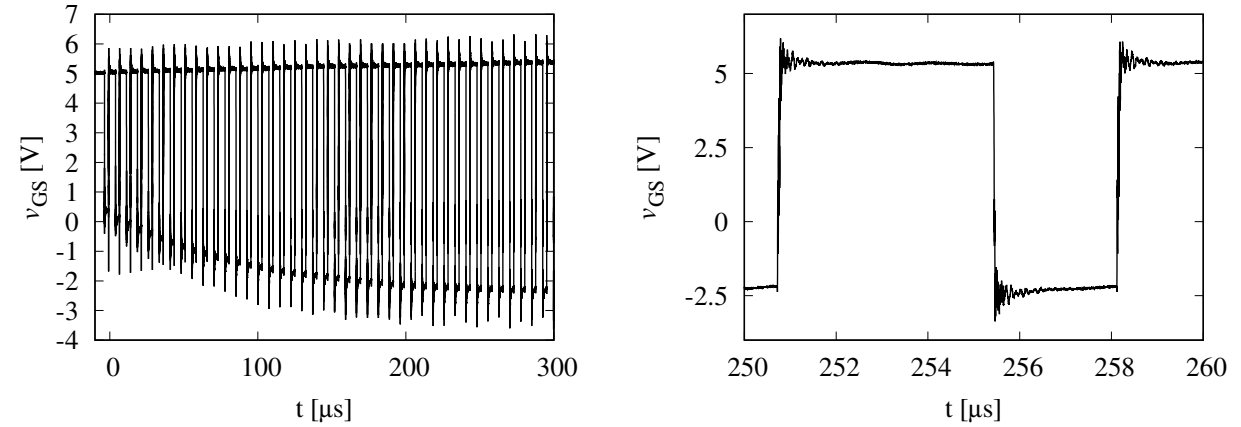


Fig. 7.3: Progression of the gate-source voltage and magnification of a cycle during steady state.

Both effects, the charging of C_{on} and discharging of C_{off} are due to the current i_{ind} which is created by T_{FF}. Especially its influence on the progression of the voltage V_{Doff} is essential for the presented concept. The current i_{ind} which can be seen in figure 7.5 is responsible for the discharging of C_{off} during turn on of the power semiconductor Q. This current was measured with an additional 1 Ω resistor in series to the transformer T_{FF}. This additional impedance is slightly reducing the charge transported by T_{FF} Q_{TFF}. This charge is the integral of the current i_{ind} during turn on and is also

shown in the same picture. Especially the ringing of i_S as well as the leakage inductance of T_{FF} can result in a noticeable extension of the discharging period. The duration of the first current gradient during turn on was about 7 ns, which was determined by the first voltage drop in v_{DS}, compare figure 3.2. The current i_{ind} on the other side is induced for around 30 ns.

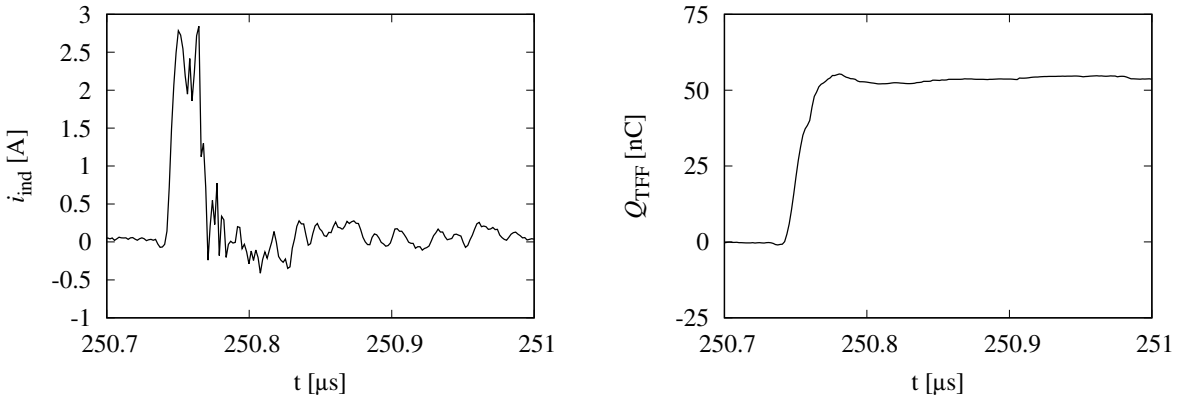


Fig. 7.4: The discharging current i_{ind} as well as the charge Q_{TFF} during turn on for $I_L = 15$ A.

Due to the current i_{ind}, Q_{TFF} is removed from C_{off} resulting in a voltage drop of:

$$dv_{Doff} = \frac{Q_{TFF}}{C_{off}} = \frac{54\,\text{nC}}{100\,\text{nF}} = 0.54\,\text{V}. \tag{7.1}$$

The trend for the voltage v_{Doff} over C_{off} is shown in figure 7.5 after achieving a steady state. The capacitor C_{off} is showing a square wave created by the discharging during turn on and charging during turn off. The discharging is due to the transformer T_{FF} and the charging due to the gate charge which is transferred onto C_{off}. Both events are highlighted in the magnification.

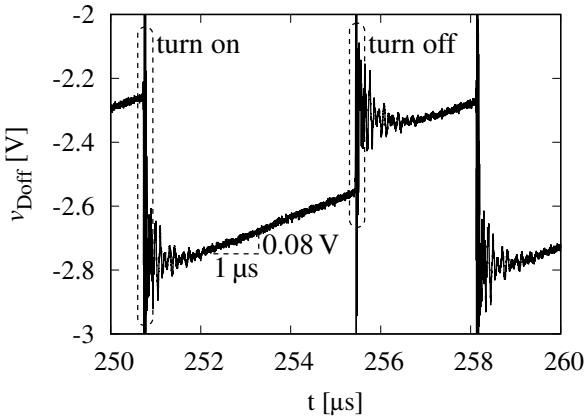


Fig. 7.5: Magnification of a cycle of v_{Doff} during steady state and the discharging current i_{ind}.

Furthermore, C_{off} is charged during on and off state with a constant current of:

$$I_{driver} = C_{off} \cdot \frac{dv_{Doff}}{dt} = 100\,\text{nF} \cdot \frac{80\,\text{mV}}{1\,\text{µs}} = 8\,\text{mA}. \tag{7.2}$$

This is exactly the basic supply current of the gate driver, labeled in the data sheet as (output supply) active current, which needs to be taken into account. Especially for low f_{sw}, this current results in a substantial charge created by the gate driver Q_{GD}.

$$Q_{\mathrm{GD}} = \frac{I_{\mathrm{driver}}}{f_{\mathrm{sw}}} = \frac{8\,\mathrm{mA}}{230\,kHz} = 35\,\mathrm{nC}. \tag{7.3}$$

The amplitude of the overall ripple dv_{Doff} over C_{off} can be adjusted by the capacitance. However, a lower ripple results in a longer settling time and therefore a trade off is necessary. In this concept, V_{Doff} describes the voltage v_{Doff} right after turn off.

Up to now only the operation under a high load current of 15 A is analyzed. A limitation of the simplified setup is the resistor in series with L_{DP} which is not depicted in the schematic of figure 7.1. The voltage drop over the resistor reduces the current gradient of I_{L} during on state for increasing load currents, which can be seen in figure 7.2. Therefore, the switching frequency was adjusted to keep the current ripple of 1 A constant for every operation point. This can be seen in figure 7.6 for a load current of 10 A and the accompanying switching frequency of 210 kHz as well as for the load current of 15 A in combination with a switching frequency of 150 kHz. This also highlights a benefit of the presented concept: Because the capacitor C_{off} is only charged during turn off and discharged during turn on, the duty cycle and switching frequency can be varied without influencing the final V_{Doff}. The switching frequency only influences the settling time which is necessary to achieve a steady V_{Doff}. Furthermore, the charge Q_{GD} can be changing and thereby have an influence on V_{Doff}. However, only the load current and the current gradient during turn on influences the amount of charge removed from C_{off}. Therefore, the focus was put on a constant current ripple to be able to compare the different operation points and the settling time was skipped.

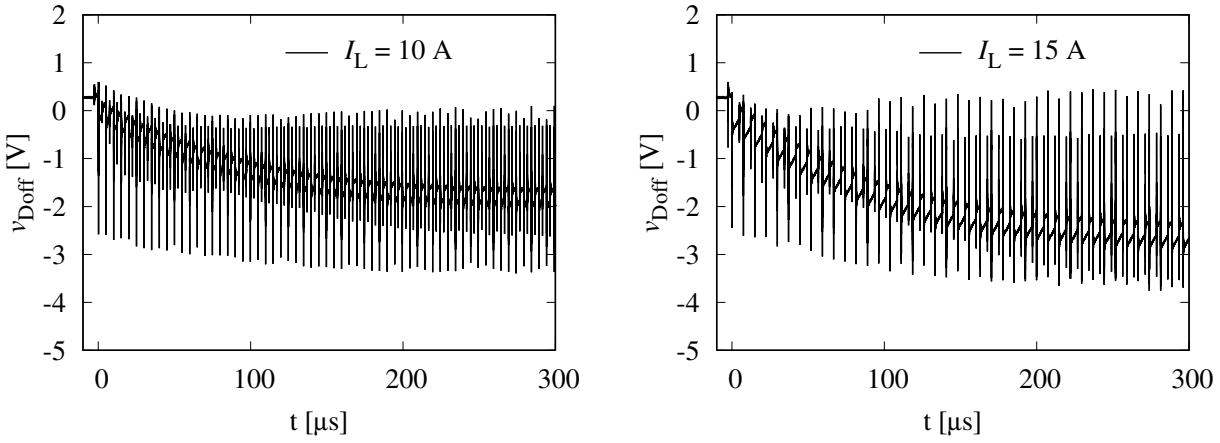


Fig. 7.6: Trend of the voltage over C_{off} while beeing discharged with different load currents and switching frequencies (210 kHz for $I_{\mathrm{L}} = 10$ A and 150 kHz for $I_{\mathrm{L}} = 15$ A).

To see the influence for different load currents, the current was swept down to 1 A in an 1 A interval. The trend of v_{Doff} for an increasing load current can be seen in figure 7.7. Two different operation areas can be distinguished. For low load currents the voltage over C_{off} is consistent with the forward voltage of D_0. The condition for this operation area is that the charge transported onto C_{off} is higher than the discharging by T_{FF}.

$$v_{\mathrm{Doff}} = v_{\mathrm{D0,FWD}} \quad \text{for} \quad Q_{\mathrm{TFF}} < Q_{\mathrm{G}} + Q_{\mathrm{GD}}. \tag{7.4}$$

An important requirement for this condition is that the additional current pulse due to the discharging of Q_{G} does not create a significant increase in voltage due to the resistor R_0. The gate charge of the applied semiconductor is an average amount of 4.5 nC when charged from 0 to 6 V. However, once the condition in equation 7.4 is surpassed, the second operation area is active. If Q_{TFF} is greater than Q_{G} and Q_{GD}, C_{off} is discharged. Thereby, Q_{G} increases because a higher voltage difference is applied to the gate until an equilibrium is achieved between the charges and Q_{TFF} = Q_{G} + Q_{GD}. Q_{TFF} is reaching a maximum for high load currents, limiting the minimal v_{Doff} created by the transformer. This is due the maximum voltage which can be created by the transformer with a fixed current gradient. The measurements are taken in a 1 A interval which explains the hard edge in the progression.

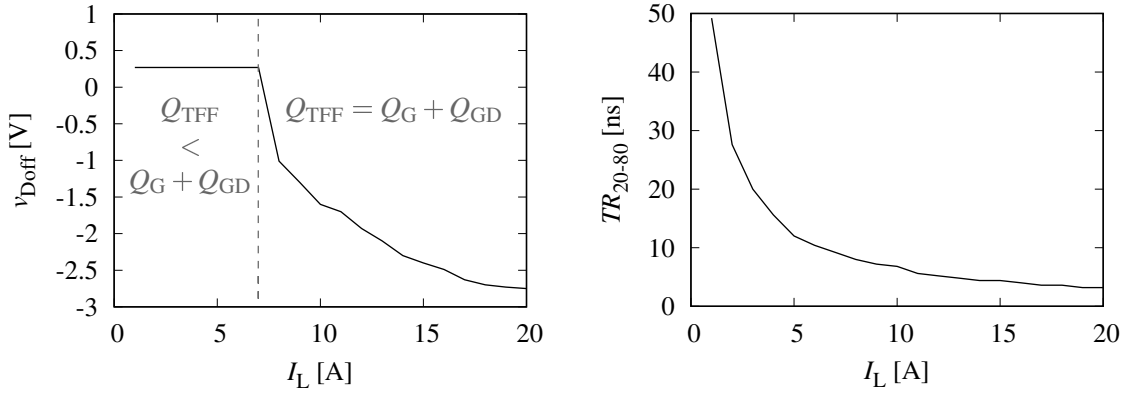


Fig. 7.7: Progression of the negative bias voltage and related rise time TR_{20-80} of v_{DS}.

A drawback of the concept is, that the negative voltage is only created above a certain load current. However, for low load currents a negative bias voltage is not always necessary. The rise time TR_{20-80} of v_{DS}, determined between 20% and 80% of the supply voltage V_{sup} is shown for the same load current range as v_{Doff} in figure 7.7. The rise time is high during low load conditions due to the C_{OSS} of the semiconductor. The slew rate is often the highest between 20% and 80% of the supply voltage V_{sup} for a semiconductor controlled by a conventional gate driver. The high rise time therefore correlates with a low slew rate which limits the miller current and prevents a

Miller-induced turn on. The transformer has therefore be fitted to the semiconductor to achieve a negative bias voltage before the slew rate becomes critical due to a low rise time.

It has to be noted that the charges Q_{TFF} as well as Q_G and Q_{GD} are only constant for every operation point defined by I_L. Q_{TFF} depends directly on the load current and rises for increases I_L. Q_G is enlarged once the delta of V_{Don} and V_{Doff} growth. Both bias voltages are influenced for higher load currents as shown in figure 7.3. Finally, Q_{GD} directly correlates to the switching frequency due to the active current of the gate driver. The transition between the two operation areas in figure 7.7 can therefore also be adjusted by manipulating these charges. Thereby the progression of the negative bias voltage can be fitted to the rise times in the application. However, the method is especially useful for high switching frequencies since Q_{GD}. Furthermore, semiconductor with a low Q_G are beneficial since a lower Q_{TFF} is necessary. This reduces the necessary i_{ind} and thereby the transformer T_{FF} can become smaller.

Applications with a high dynamic are still critical for the presented design because of the settling time which is necessary to attain the final negative bias voltage necessary to achieve a safe turn off for high load currents. Intelligent control mechanisms could be used to prevent an early increase of the load current. Another solution could be a three stage gate driver, charging Q_G + Q_{GD} to another potential. Overall, the measurements have shown that the concept is suitable to prevent Miller-induced turn on if designed appropriate.

8 Summary and outlook

In the course of this work, a novel simple design for a coreless transformer was developed. The two-layer design is suitable for various substrates, especially printed circuit boards. It is optimized to achieve a high magnetic coupling with an adjustable transformation ratio and a low primary inductance. Special attention was given to the coupling capacitance to simultaneously realize a wide bandwidth. The relative permittivity of the separator material is identified as a factor by which the capacitance could be adjusted without affecting the magnetic coupling. Based on a simple equivalent circuit an equation which can be used to estimate the first resonant frequency, and thereby the bandwidth, was introduced. The lumped element model of the transformer was extended to also cover the effect of eddy currents and realize an accurate simulation up to the first resonant frequency.

The aim of these optimizations was to achieve an especially suitable transformer for the IFF method. The IFF method uses a transformer to induce an additional voltage into the gate loop and thereby accelerate transitions during hard switching. The low primary inductance of the transformer design does not significantly increase the inductance of the commutation loop and thus prevents higher over-voltage peaks during turn off. Due to the high bandwidth the induced voltage is maximized. The inductance of the secondary winding as well as the coupling capacitance is lower than in previous multi layer transformer designs which reduces the ringing of the gate loop triggered by the IFF method and miller currents. Overall, the new design was successfully used to reduce the turn-on losses of a SJMOSFET by 24 % at the maximum continuous drain current compared to the conventional approach. For the gate driver only a positive bias voltage of 12 V was used for both designs with a single gate driver output for turn on and turn off. The impact of the additional transformer could be further reduced compared to previous transformer designs, so that it does not influence the turn-off transition. Even though simulations also suggested a reduction of the turn-off losses by the IFF method compared to the conventional approach, this could not be verified up to the maximum continuous drain current. However, the maximum over-voltage peak was identified as an indication above which load current the IFF method could be effective to reduce the turn-off losses. Again, a comparison to the conventional approach is necessary to see a distinction of the over-voltage peak above the critical load current.

In addition to the new transformer design, the work introduces improvements to the IFF method. An additional freewheeling diode in parallel with the primary winding of the transformer was suggested for devices with a low threshold voltage. The benefits of the diode for a safe turn off are shown with a GaN HEMT as an example. Furthermore, the necessity of a rectifier at the secondary winding was shown for GaN GITs. For these devices the IFF method only lowers the turn-on losses above a certain load current compared to the conventional gate driving approach. Although the IFF method also enables a safe turn on for even higher load currents than the conventional approach.

New insights into the impacts of the IFF method are also presented. Based on a boost converter, the effect of the method on the EMI was measured and compared to the conventional gate driving approach. Two different boost converter setups are compared, one with a 330 µH inductor and another with 100 µH. Because of the higher efficiency gain due to the lower current ripple, the 330 µH setup was used for the EMI comparison. At an output current of 1 A and an output voltage of 380 V the efficiency was increased from 96 % to 96.3 % for this setup, which corresponds to a loss reduction of around 1 W. At this operation point, the conducted emissions of the boost converter do not change between the conventional approach and the IFF method. This is different for the radiated emissions which increase due to the higher current gradient and especially the over-current peak. The greater radiated emissions have to be considered if the IFF method is applied to applications with a low limit. For these applications, the NIFF method can be a solution. By changing the polarity of the secondary winding, the switching is slowed down and therefore also the EMI will be reduced. This approach was demonstrated on an IGBT which also can be accelerated by the IFF method if a magnetic core is used to increase the output voltage of the transformer. Since the focus of this work is on the coreless transformer, the IGBT is used to show that the design is depending on high current gradients if the primary inductance should be kept small. Another aspect of this work is the use of the IFF method on parallel connected power semiconductors. Again, in comparison to conventional gate drivers, the new approach is particularly beneficial for the turn-on losses due to shorter transition times. Furthermore, a parallel use of the IFF method can prevent current asymmetries from increasing at higher load currents. Moreover, a cross-coupling of the feedback transformers results in a uniform loss distribution along the semiconductors.

Since the new design of a coreless transformer is optimized for hard-switching applications, it also is suitable for applications other than the IFF method. The transformer can be used similar to a Rogowski coil as a current sensor to characterize the high current gradients during switching. With a simple filter and integrator stage added to the transformer, a high bandwidth of 100 kHz

up to 200 MHz was realized. Even though for frequencies above 90 MHz the phase shift should be taken into account. Another application for the transformer design introduced in this work is the generation of an isolated bias voltage. The approach is particularly advantageous if a negative bias voltage is necessary, for example, due to a low threshold voltage. The negative voltage is only created above a certain load current. However, due to the higher rise time, and therefore reduced influence of C_{GD}, a negative bias voltage is not always necessary for low load currents.

Outlook

The benefits of the new transformer design have been shown, especially for PCB substrates. Since the design is particularly suitable for integration into a power module, the application into more suitable substrates could be advantageous. Thereby, the different approaches presented in this work could be directly added to the power module to realize additional functions or easier control.

For the presented current sensor in chapter 5, an extension of the circuit by a tunnel magnetoresistance sensor or Hall effect sensor could increase the frequency range down to DC. A smaller transformer could also increase the upper frequency limit if the signal conditioning circuit is adapted. Nevertheless, this would also reduce the magnitude of the signal and thereby increase the influence of noise which are the restrictions of this approach.

In chapter 6.1 the novel design was successfully used to apply the IFF method on a SJMOSFET. It is worth mentioning that the maximum gate voltage in figure 6.2 still has a safety margin of 30 V - 14 V = 16 V from $V_{GS,max,dyn}$. By increasing the overlap area X1 and length X of the transformer (eg. figure 4.2(a)), this safety margin can be reduced. Thereby the turn-on losses could be decreased by more than the current 24 % at the maximum load current. To clarify the effects of the IFF method on turn off, it would be insightful to look into devices with a lower C_{OSS} like GaN HEMTs. Furthermore, the high radiated emissions could be reduced by combining the IFF method with slope shaping approaches. The challenge would be to achieve comparable radiated emissions and still achieve a significant reduction of the dynamic losses.

In chapter 6.5, the IFF method was used on parallel connected power semiconductors. The preceding four-layer design was used in combination with GaN HEMTs which resulted in high current gradients and ringing and therefore challenging measurements. Using the novel design would dampen the oscillations and using SJMOSFETs could further help to illustrate the benefits and focusing on the method due to the slower current gradients and reduced oscillations which can simplify the measurements.

The example circuit realizing the negative bias voltage in chapter 7 still has a high settling time to attain the final voltage level. Since the voltage can be necessary to achieve a safe turn off for

high load currents, this can be critical for applications with a high dynamic. Intelligent control mechanisms could be used to prevent an early increase of the load current. Another solution could be a three stage gate driver, charging $Q_G + Q_{GD}$ to another potential for load currents with a high rise time.

Furthermore, it could be worthwhile to combine the NIFF method from chapter 6.6 with the negative bias voltage in chapter 7. If a slow settling time is realized, the EMI of a traction inverter could be optimized. By using the NIFF method, the duration of the turn-off transition can be controlled by the negative bias voltage. This voltage can be adjusted according to the load current with the approach of chapter 7. By combining the two approaches, the EMI generated by the turn-off transition can now be shifted over several frequencies for the different load currents switched to generate the current sine wave for the electric motor. The result could be a broader EMI spectrum with a lower overall peak in the frequency domain influenced by the current slope. However, because the turn-on transition would still be constant, this could limit the impact of this concept.

Appendix

A Component values of the measurement setups

Most of the critical parts in the double pulse setup are kept the same for all the different measurements. The chip SI8271GB-IS was used as a gate driver [156]. The inductor L_{DP} was a self wound coil with an inductance of 463 µH. The diode IDL12G65C5 was used as free wheeling diode D_{FWD} [157]. However, especially the gate driving concepts as well as the component values inside the gate loop differ for the various considered power semiconductors. In this chapter the explicit values of the critical components will be listed.

A.1 Current sensor

The model parameters of the current sensor in chapter 5.2:

L_P	k_{PS}	L_S	R_P	R_S	C_P	C_S	C_K
1.3 nH	0.4	42 nH	6 mΩ	220 mΩ	4 pF	3 pF	7 pF

Table A.1: Model parameters of the coreless PCB transformer used for the current sensor.

Model parameters of the signal conditioning circuitry in chapter 5.2:

R_{LP}	C_{LP}	C_i	R_1	R_2	R_3	R_4
30 Ω	30 pF	100 pF	30 Ω	20 kΩ	180 Ω	75 Ω

Table A.2: Model parameters of the signal conditioning circuitry.

A.2 GaN GIT driving circuit

The gate loops in chapter 6.3 are characterized with the following component values. For the IFF method the transformer T_{FF} from chapter 4.2 was used.

V_{Don}	V_{Doff}	R_{Gon}	R_{Goff}	R_{Boost}	C_{Boost}
12 V	-3 V	680 Ω	20 Ω	6.2 Ω	1.5 nF

Table A.3: Conventional gate driving circuit for GaN GITs in chapter 6.3.1.

V_{Don}	V_{Doff}	R_{Gon}	R_{Goff}
5 V	-3 V	51 Ω	20 Ω

Table A.4: IFF-gate driving circuit for GaN GITs in chapter 6.3.2.

A.3 GaN HEMT driving circuit

The gate loops in chapter 6.2 and chapter 6.5 are characterized with the following component values. In chapter 6.2 for the IFF method the transformer T_{FF} from chapter 4.2 was used. In chapter 6.5 the transformer design from chapter 4.2.2 was used with a reduced distance I of only 50 µm.

V_{Don}	V_{Doff}	R_{Gon}
6 V	0/-4 V	9.2 Ω

Table A.5: Conventional gate driving circuit for GaN HEMTs in chapter 6.2 and chapter 6.5.

A.4 SJMOSFET driving circuit and Boost converter setup

For the setups using a SJMOSFET [158] in chapter 6.1 and chapter 6.4 the gate driving methods were applied according to figure 3.4. For the IFF method in chapter 6.1 the transformer T_{FF} from chapter 4.2 was used. For the boost converter setups in chapter 6.4 the mechanical dimensions of T_{FF} are as shown in table 4.1 except for X1 = 13 mm and Z = 2 mm. This results in slightly different model characteristics; cf. table A.6:

L_P	k_{PS}	L_S	R_P	R_S	C_K
2.1 nH	0.45	117 nH	9 mΩ	850 mΩ	20 pF

Table A.6: Model parameters of a variation of the coreless PCB transformer.

The boost converter is controlled by a LM3481 chip [159] set to a switching frequency of 380 kHz. In addition to a voltage divider measuring the output voltage, a 5 mΩ Shunt was added in the source contact to measure the current and utilize all the provided functionality of the controller. Furthermore, the input and output voltages are buffered with the following capacitances; cf. figure 6.16:

V_{Don}	R_G	C_{in}	C_{com}	C_{out}
12 V	2 Ω	1.5 mF	1 µF	235 µF

Table A.7: Gate driving circuit for the SJMOSFETs and boost converter capacitances.

A.5 Setup used to create a negative gate supply

For the setups in chapter 7 the same transformer T_{FF} as for the boost converter setup was used, resulting in the model characteristics in table A.6. As the semiconductor Q a GaN HEMT is used [66]. An Additional 1.2 Ω shunt is used in series with the transformer T_{FF} to measure i_{ind}, slightly reducing the induced current.

V_{Don}	R_{Gon}	R_{Goff}	R_0	C_{off}	C_{on}
5 V	15 Ω	15 Ω	20 Ω	100 nF	10 µF

Table A.8: Applied components for the concept in figure 7.1(b).

A.6 Setup used to drive the IGBT

All previous designs used the same gate driver, this was different for the IGBT setup in chapter 6.6. The main difference is, that the chip IXDD630 from IXYS was used as a gate driver in combination with an additional 2 Ω gate resistor. The high side diode of the utilized IGBT module FF200R12KT4 from Infineon was used as free wheeling diode D_{FWD}. To measure the emitter current of the characterized low side switch, the SBNC-2-01 coaxial shunt from T&M research was used.

B Measuring instruments and special signal sources

In the following the most important measuring instruments as well as special signal sources are listed and linked to their application in this work:

Double pulse measurement	oscilloscope	Lecroy HDO6104-MS
Double pulse measurement	differential probe	TESTEC TT-SI9001
Double pulse measurement	differential probe	Pico Technology TA045 & TA046
S-Parameter measurement	VNA	Agilent E5061B
Efficiency measurement	digital multimeter	Agilent 34410A
EMI measurement	signal analyzer	Agilent N9020A
EMI measurement	coupling network	LISN NNBM 8125
Current sensor characterization	signal generator	Tektronix AFG 3252C
Current sensor characterization	amplifier	Hubert A 1020

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List of Abbreviations

ADS	advanced design system
AIT	assembly and interconnection technology
Al	aluminum
AlGaN	aluminum gallium nitride
CMOS	complementary metal-oxide-semiconductor
D	drain connection
DD	drill diameter
DFN	dual-flat no-leads
D_{FWD}	freewheeling diode
D_{GS}	gate source diode
DMOSFET	double-diffused metal-oxide-semiconductor field-effect transistor
D_{SK}	Schottky diode
DUT	device under test
EM	electromagnetic
EMI	electromagnetic interference
FEM	finite element method
FR	flame retardant
GaN	gallium nitride
GIT	gate injection transistor
HEMT	high-electron-mobility transistor
HFET	heterojunction field-effect transistor
I	distance between the primary and secondary windings
IFF	inductive feed forward
IGBT	insulated-gate bipolar transistor
K	Kelvin contact
MoM	method of moments
MOSFET	metal–oxide–semiconductor field-effect transistor

N	number of secondary turns
NIFF	negative inductive feed forward
PCB	printed circuit board
PEEC	partial element equivalent circuit method
Q	discrete semiconductor
Si	silicon
SiC	silicon carbide
SPICE	simulation program with integrated circuit emphasis
SiO_2	silicon dioxide
SJMOSFET	superjunction metal–oxide–semiconductor field-effect transistor
T	copper thickness
TMOSFET	trench metal-oxide-semiconductor field-effect transistor
V	distance between the vias of the primary and secondary winding
VNA	vector network analyzer
W	width of the secondary winding
X	length of the primary winding
X1	overlap area
Y	width of the primary winding
Z	thickness of the substrate
2DEG	two-dimensional electron gas

List of Symbols

A	1	closed loop gain
A_D	1	open loop gain
C_{Boost}	F	boost capacitance
C_{com}	F	commutation capacitance
C_{DS}	F	drain-source capacitance
C_{GD}	F	gate-drain capacitance
C_{GS}	F	gate-source capacitance
C_i	F	integration capacitance
C_{in}	F	input smoothing capacitor
C_K	F	coupling capacitance
C_{on}	F	buffer capacitance for the positive gate driver supply
C_{off}	F	buffer capacitance for the negative gate driver supply
C_{out}	F	output smoothing capacitor
C_{OSS}	F	output capacitance
$C_{O(ER)}$	F	effective output capacitance
C_P	F	interwinding capacitance of the primary winding
C_S	F	interwinding capacitance of the secondary winding
$E_{turn\text{-}on}$	J	turn-on energy
$E_{turn\text{-}off}$	J	turn-off energy
f_0	s^{-1}	first resonance frequency
f_{sw}	s^{-1}	switching frequency
f_T	1	transfer function
g	1	loop gain
i_{Boost}	A	boost current
i_{CH}	A	channel current
i_D	A	drain current
i_E	A	emitter current

i_{FWD}	A	current through the forward diode
i_G	A	gate current
$i_{G,max}$	A	maximum gate current
$I_{G,max}$	A	maximum gate current limitation
$I_{G,max,dyn}$	A	maximum dynamic gate current limitation
I_{in}	A	input current
i_{ind}	A	induced current
I_L	A	load current
I_{out}	A	output current
i_S	A	source current
i_{SM}	A	measured source current
i_{UP}	A	boost converter inductor current
k	1	coupling coefficient
k_f	1	preamplification
k_r	1	feedback factor
L_{CS}	H	common source inductance
L_D	H	inductance of the drain connection
L_{DP}	H	inductor of the double pulse test setup
L_G	H	inductance of the gate connection
L_K	H	inductance of the Kelvin connection
L_M	H	mutual inductance
L_P	H	inductance of the primary winding
L_S	H	inductance of the secondary winding
L_{setup}	H	parasitic inductance of the setup
L_{UP}	H	inductor of the boost converter
P_{MOS}	W	active power
P_{out}	W	output power
Q_G	C	gate charge
Q_{GD}	C	charge created by the gate driver
Q_{rr}	C	reverse recovery charge
Q_{TFF}	C	charge transported by T_{FF}
R_0	Ω	resistance to define the initial voltage
R_{Boost}	Ω	boost resistance
R_{DSon}	Ω	on-state resistance
R_G	Ω	gate resistance

R_{Goff}	Ω	gate resistance in series with the negative bias voltage
R_{Gon}	Ω	gate resistance in series with the positive bias voltage
R_{P}	Ω	resistance of the primary winding
R_{S}	Ω	resistance of the secondary winding
t_0	s	transition time
t_{n}	s	negative integration time
t_{p}	s	positive integration time
T_{FF}	1	feed-forward transformer
TR_{20-80}	s	rise time
t_{tr}	s	transition time
v_{CE}	V	collector-emitter voltage
v_{D}	V	pulsed gate driver voltage
V_{Doff}	V	negative bias voltage
V_{Don}	V	positive bias voltage
v_{DS}	V	drain-source voltage
v_{DSI}	V	internal drain-source voltage
$V_{\mathrm{DS,max}}$	V	maximum drain-source voltage
$V_{\mathrm{GS,max}}$	V	maximum gate-source voltage limitation
$V_{\mathrm{GS,max,dyn}}$	V	maximum dynamic gate-source voltage limitation
v_{GS}	V	gate-source voltage
v_{GSI}	V	internal gate-source voltage
v_{ind}	V	induced voltage
v_{m}	A	measured induced voltage
V_{meas}	V	measurement voltage
V_{out}	V	output voltage
V_{sup}	V	supply voltage
v_{SW}	V	switching potential
V_{th}	V	threshold voltage

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List of Publications by the Author

- J. Hackel, A. Seidel, J. Wittmann, and B. Wicht, "Capacitive gate drive signal transmission with transient immunity up to 300 V/ns," ANALOG 2016; 15. ITG/GMM-Symposium, Bremen, Germany, 2016, pp. 1-5.
- J. Hackel, M. Ebli, and M. Pfost, "A novel gate driving approach to balance the transient current of parallel-connected GaN-HEMTs," CIPS 2018; 10th International Conference on Integrated Power Electronics Systems, Stuttgart, Germany, 2018, pp. 1-4.
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