Research Article

Transfer-free graphene passivation of sub 100 nm thin Pt and Pt–Cu electrodes for memristive devices

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Abstract
Memristive switches are among the most promising building blocks for future neuromorphic computing. These devices are based on a complex interplay of redox reactions on the nanoscale. Nanoionic phenomena enable non-linear and low-power resistance transition in ultra-short programming times. However, when not controlled, the same electrochemical reactions can result in device degradation and instability over time. Two-dimensional barriers have been suggested to precisely manipulate the nanoionic processes. But fabrication-friendly integration of these materials in memristive devices is challenging.Here we report on a novel process for graphene passivation of thin platinum and platinum/copper electrodes. We also studied the level of defects of graphene after deposition of selected oxides that are relevant for memristive switching.

Article Highlights

- Direct Graphene growth on ultra thin Pt and Pt-Cu Layers.
- Optimised Adhesion Layer for CVD growth.
- Deposition of Oxides on Graphene by ALD, PECVD and PVD.

Keywords Chemical vapor deposition · CVD · Graphene · 2D material · Heterostructure · Adhesion layer · Memristive switching

1 Introduction

Mobile applications and portable devices rely on dense solid-state memory devices, which today are dominated by non-volatile Flash technology [1]. Flash is based on floating gate transistors. Despite their low-energy working principle (for NAND Flash), Flash suffers from a number of drawbacks, including slow programming speed, high programming voltages and low device endurance [2], which hinders its application in logic-in-memory [3] (beyond von Neumann) and neuromorphic computing architectures [4]. Resistively switching random access memories (RRAMs), also known as memristive switches, are based on nanoionic redox reactions and are among the most promising alternatives to replace conventional Flash memories [2]. RRAMs have a high application potential for storage-class memories [5], memory-intense logic [3, 6, 7] and neuromorphics [8–11].

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RRAMs are two-terminal thin-film devices, where the resistance of a memristively switching insulator can be tuned between at least two stable resistance values (OFF and ON, or high resistive, HRS, and low resistive, LRS, state), which encode at least two logic states. This resistance transition is attributed to a tuneable arrangement of mobile ions. There are two important classes of RRAMs: (I) Valance Change Mechanism (VCM) memories are based on the drift of mobile oxygen vacancies in transition metal oxides, which results in the formation of sub-stoichiometric phase(s). These phase(s) allow for example for manipulation of a Schottky barrier between the electronically conductive sub-stoichiometric phase(s) and a high work function electrode [12, 13]. (II) Electrochemical Metallization cells (ECM, also known as Conductive Bridge RAM, CBRAM), are based on mobile metal cations that can form a nanoscale metallic filament, which bridges the device's terminals [14]. For ECM cells, Cu and Pt are common materials for the anode and cathode side, respectively [15]. While VCM cells offer high endurance and ease of integration in CMOS processes, ECM devices have attracted high attention due to their ultra-low power operation (scalable down to 10 fJ/bit) [16] and ultimate scalability reaching the atomic level [17–21]. In addition, the large resistance ratio between the ON and OFF state (typically 1000 or even higher) is of particular importance for integration of RRAMs in dense memory arrays [22]. A significant drawback of ECM devices is their inferior device stability and endurance. Degradation of the switching characteristics and the resistance levels are attributed to unintentional internal ionic redox reactions and chemical diffusion of the mobile cations [23, 24]. Conventional diffusion barriers such as silicon nitride thin-films (thickness typically 2–5 nm) result in large voltage drops across the barrier, which hinders low-voltage and thus low-power operation. In contrast, ultra-thin or even atomically thin materials like graphene mono- or multilayers (thickness typically $\ll 2$ nm) have been suggested for passivation of the device's electrodes to overcome this drawback. First results demonstrate that the integration of graphene significantly affects the switching behaviour not only for ECM-type devices but also for VCM cells [25, 26]. For example, M. Lübben et al. demonstrated that graphene can be used as a diffusion barrier for Ag, to prevent intermixing of the active electrode (Ag or Cu) and the memristively switching insulator [25, 27]. Lee et al. reported on the role of graphene as oxygen ion blocking layer, which improved the device performance (e.g. the resistance window) and allowed for systematic tuning of the switching behaviour [26].

The most industry relevant method to grow 2D materials is chemical vapor deposition (CVD) [28]. CVD allows for high-quality and large-area growth of 2D materials [29] like graphene and hexagonal boron nitride (2D h-BN) particularly on transition metal catalysts like copper [30, 31] and nickel [32–34]. The typical process flow relies on a sacrificial growth substrate, e.g. foil or epitaxial wafer [35, 36], that is optimised for the CVD process. The typical thickness of these catalysts is in the range of a few tens or even hundreds of micrometres. For applications this requires subsequent layer transfer [37, 38], which remains challenging, especially if like in the case of RRAM scalability and reproducibly, clean interfaces are required. This heterogeneous interfacing challenge is common across all 2D materials including less crystalline and amorphous films. In line with established methods for mass-production in microelectronics, transfer-free, direct growth of a 2D layer into a device structure would be highly advantageous and desirable. However, this heavily constrains the CVD process parameter space, and thus direct integration remains largely inaccessible, even for applications like RRAMs where the device stack contains Cu (anode) or Pt (cathode). Thermal CVD processes typically rely on process temperatures of 600 °C and more for at least tens of minutes. This makes direct integration of 2D materials in RRAMs challenging due to the well-known dewetting of thin metal electrodes. In this context, 2D materials have been grown on Ni and Cu catalyst layers as thin as 150 and 500 nm [39–42]. However, these layers are yet too thick for electrode fabrication of devices with dimensions at the sub 100 nm technology node. Very recently, Y. Hagendoorn et al. reported on the growth of graphene on SiO_2 underneath a 50 nm thick seed layer of Pt [43]. After graphene growth, the Pt layer has been removed (e.g. by wet-chemical etching). Therefore, the work by Hagendoorn et al. did not focus on graphene passivation on thin Pt electrodes and it is not clear if the Pt layer dewetted after CVD growth.

Here, we focus on a novel direct integration process for 2D materials in ECM cells, and demonstrate that the dewetting of 30–90 nm thin Pt and Pt–Cu electrodes can be effectively suppressed during high temperature graphene CVD via the design of an optimised adhesion layer. We analyse the feasible electrode quality not only after graphene CVD, but we also studied the impact of oxide deposition on graphene of selected oxides, including SiO_2, Ta_2O_5 and Al_2O_3, which are relevant for memristive switching. We discuss the potential of this approach for future direct heterogeneous materials device integration approaches for RRAM technology.

2 Experimental details

We utilise TiO_2 as a high-temperature adhesion layer for ultra-thin metal electrodes prepared by an optimised process that has been originally used for the fabrication of

ferroelectric thin-films [44, 45]. A *p*-doped Si wafer is used and wet-oxidised to form a 450 nm thick SiO_2 layer. Afterwards, a TiO_2 adhesion layer is prepared by direct-current (DC) magnetron-sputtering of 10 nm Ti and oxidation in a diffusion furnace (temperature 700 °C in O_2 for 10 min). The Pt thin-film (thickness 30–100 nm) is then DC sputtered at a substrate temperature of 150 °C. For sputtering of Ti and Pt a 4″ von Ardenne Cluster Tool 500 ES was used. The sputtering power was set to 300 W with an Ar mass flow of 30 sccm (pressure $5.4{\cdot}10^{-3}$ hPa). Next, the platinised samples were annealed in N_2 at 800 °C for 5 min by rapid thermal annealing (RTA, STEAG AST SHS100MA). In addition to Pt samples, samples with Pt–Cu heterostructures were also fabricated. In this case, 30–100 nm Pt thin-films were deposited on $Si/SiO_2/TiO_2$ substrates based on the process described above. Subsequently, 60 nm Cu were thermally evaporated (rate 0.07 nm s^{-1}).

Graphene CVD was carried out on both Pt and Pt–Cu samples at 800 °C using a commercial cold-wall reactor (Aixtron BM Pro). A CH_4 flow rate of 1 sccm and a H_2 flow rate of 26 sccm were used at a total pressure of 50 mbar. For selected samples a growth temperature of 920 °C was used. The growth time depends on the nucleation density, i.e. nucleation sites for graphene growth on the catalyst such as impurities, grain boundaries etc. The smaller the nucleation density, the larger the potential grain size of graphene. However, a small nucleation density requires a long process time of several minutes to hours to form a fully covering film. Based on previous growth experiments on Cu foils we chose a growth time of 2 h. The process flow for graphene growth on Pt and Pt–Cu samples is schematically summarised in Fig. 1a, b, respectively.

To study the impact of oxide deposition on graphene, SiO_2 and Ta_2O_5 were electron-beam (e-beam) evaporated in ultra-high vacuum (10^{-8} hPa) with an evaporation rate of 0.01 nm s^{-1} using the von Ardenne Cluster Tool 500 ES. In addition, SiO_2 was deposited by plasma enhanced CVD (PECVD) using an Oxford PlasmaLab 80Plus system (2% SiH_4 in He, flow rate 192 sccm, N_2O flow rate 355 sccm, 50 W plasma power, pressure 1.33 hPa, deposition temperature and time 350 °C and 30 s, respectively). For comparison, Al_2O_3 was also deposited on transferred graphene using an ozone based atomic layer deposition (ALD) process as described in Ref. [46]. In all cases, the oxide layers were deposited after transfer of graphene on Si/SiO_2. Moreover, graphene grown on selected Pt thin-films has been transferred on oxidised Si samples for further characterization. For transfer we used a bubbling transfer process in all cases as described in Ref [38].

For scanning electron microscopy (SEM) a Carl Zeiss SIGMA VP SEM (1.5–2 kV) was used. Energy dispersive X-ray spectroscopy (EDX) was done using a FEI Philips XL30 sFEG SEM. Raman spectroscopy was performed using a 532 nm laser. For atomic force microscopy (AFM) a Digital Instruments Dimension 3100 AFM under tapping mode at a scanning frequency of 1 Hz was used.

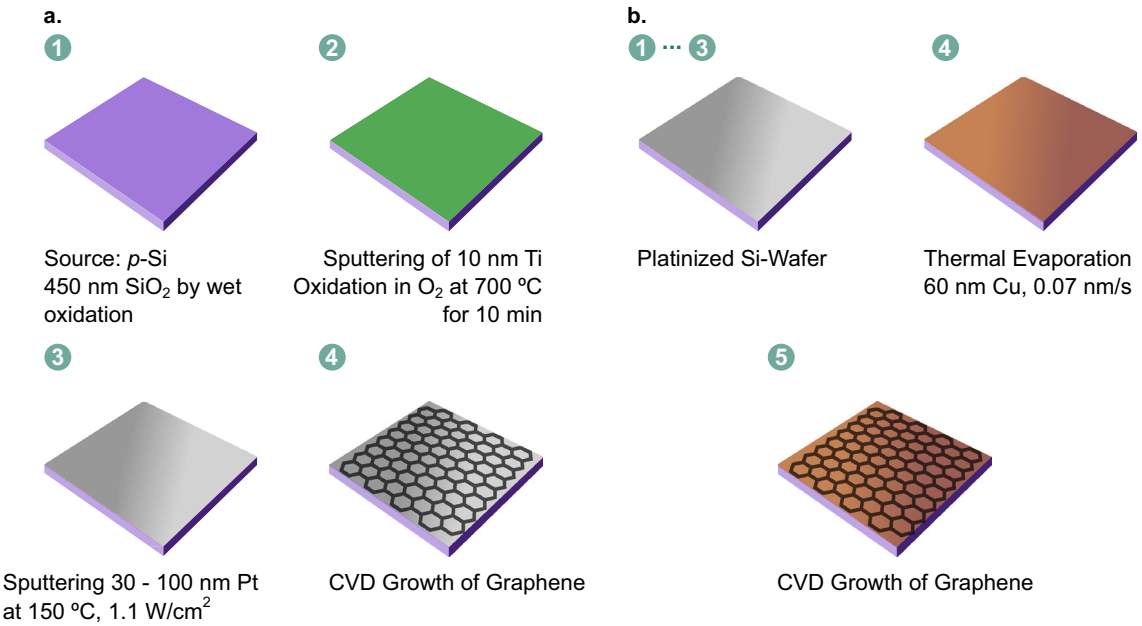

Fig. 1 Schematic process flow for graphene growth on **a** Pt and **b** Pt–Cu thin-films. Labels (1)–(5) indicate individual process steps such as Pt sputtering or Cu thermal evaporation

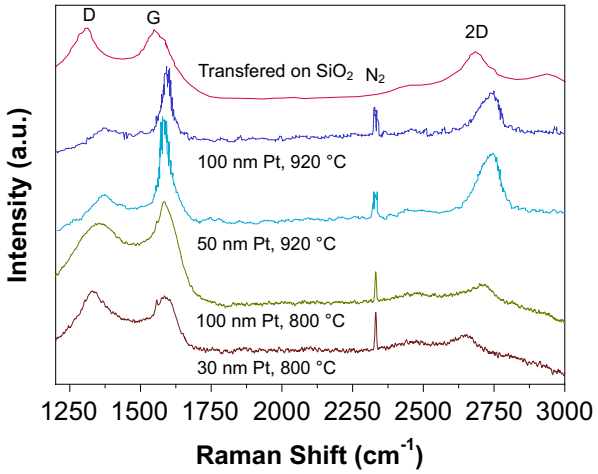

Fig. 2 Raman spectra of graphene grown at 800 °C on 30 nm Pt (red) and 100 nm Pt (green) thin-films and grown at 920 °C on 50 nm Pt (cyan) and 100 nm (purple) thin-films. The Raman spectrum (magenta) of graphene grown on 50 nm Pt (growth temperature 800 °C) and transferred an oxidized Si wafer is shown for comparison

3 Results and discussion

3.1 Graphene growth on Pt thin-films

Figure 2 depicts Raman spectra of graphene deposited on Pt films with a thickness from 30 to 100 nm. We did not observe any dewetting of the catalyst layers for a growth temperature of up to 800 °C. The G peak in the spectra at 1582 cm^{-1} and 2D (sometimes called G′) peak (at about 2720 cm^{-1}) are the fingerprint of graphene, whereas the D peak (around 1350 cm^{-1}) is related to defects [47]. The peak at 2325 cm^{-1} is attributed to atmospheric N_2 during the measurement and hence not affected by the quality of the graphene layer. It is thus a good reference to ensure that any peak shift is not resulting from a simple measurement artefact [48]. The G and 2D peaks clearly show that in all cases, i.e. at 800 °C and 920 °C (Fig. 2), graphene has been deposited. Note, the signal to noise ratio of the characteristic Raman peaks of graphene measured directly on Pt thin-films is weak. Therefore, we used a moving average filter over 5 data points. For comparison, graphene grown on 50 nm Pt (at 800 °C) has been transferred onto a Si/SiO_2 sample (magenta spectrum in Fig. 2). The signal to noise ratio was found to be much higher for transferred graphene on SiO_2 compared to graphene on Pt. It is noteworthy that the 2D peak and D peak are blue-shifted by 20–65 cm^{-1} for graphene grown on 30 nm Pt and the transferred graphene, while for the growth on 50 and 100 nm Pt at 920 °C we observe a red-shift of the 2D peak (while no other shifts are observed). This is potentially due to strain on graphene induced by the catalyst [49].

The D/G-ratio for the 30 nm Pt catalyst was found to be 1 and 0.8 for the 100 nm Pt thin-film. This is approximately three times lower compared to what has been reported by Hagendoorn et al. [43]. According to literature, the D/G-ratio is usually between 0 and 10 [50]. This means that the films have a relatively high defect concentration. However, there is no clear trend between the D/G-ratio and the catalyst layer thickness. For example, for 50 nm thick Pt layers (not shown here) we measured a D/G-ratio of 0.57 and for a different sample with 100 nm thick Pt a D/G-ratio of 0.63 was measured. The transferred sample has a D/G-ratio of 0.65. The large D/G-ratio can be reduced by higher growth temperatures. For example, at 920 °C on 50 nm and 100 nm Pt thin-films we measure a D/G-ratio of 0.28 and 0.37 (thus, more than six times lower compared to the results reported by Hagendoorn et al. [43]), respectively.

Microscopy images were taken to analyse the surface morphology of the as-grown graphene layers and transferred graphene. Figure 3a exemplarily shows a SEM image of a graphene layer grown on 100 nm Pt. On the microscale at least three different features in light grey, grey and dark grey can be identified, which are highlighted by (A), (B) and (C). The greyscale contrast indicates the growth of few (B) to multi-layer graphene (C). Figure 3a also reveals that only micrometre-scale graphene grains were formed during growth. This is about one to two orders of magnitude smaller to graphene flakes grown on conventional Cu tapes based on the CVD growth process described above [28]. According to atomic force microscopy (Fig. 3b), a roughness of 1.4 nm rms was measured on the microscale, which is comparable to the roughness of the Pt thin-films before graphene growth (this has been previously measured and reported e.g. in Refs. [51, 52]). Note, this is an order of magnitude smoother compared to the roughness reported by Hagendoorn et al. [43], which is important for subsequent deposition of thin oxides for fabrication of memristive devices. In the AFM image graphene grains are hardly visible, thus we conclude that the thickness difference between the grains is below the surface roughness. Consequently, (A) in Fig. 3a is a single layer of graphene (thickness ≈ 0.3 nm), and (B) and (C) would correspond to maximum 2–4 graphene layers. The small graphene grain size can be explained by the grains of the polycrystalline Pt thin-films which are of similar size. We believe that graphene nucleation is facilitated at the Pt grain boundaries. The existence of multilayer graphene ((C) in Fig. 3a) can be explained by grain boundary facilitated growth and is in agreement with the Raman spectra (Fig. 2), where relatively broad 2D peaks were measured. Consequently, there will be areas with mono-, few and multilayers of graphene when a film fully covering the catalyst is grown.

Due to the poor optical and material contrast between graphene and Pt, graphene grown on selected Pt

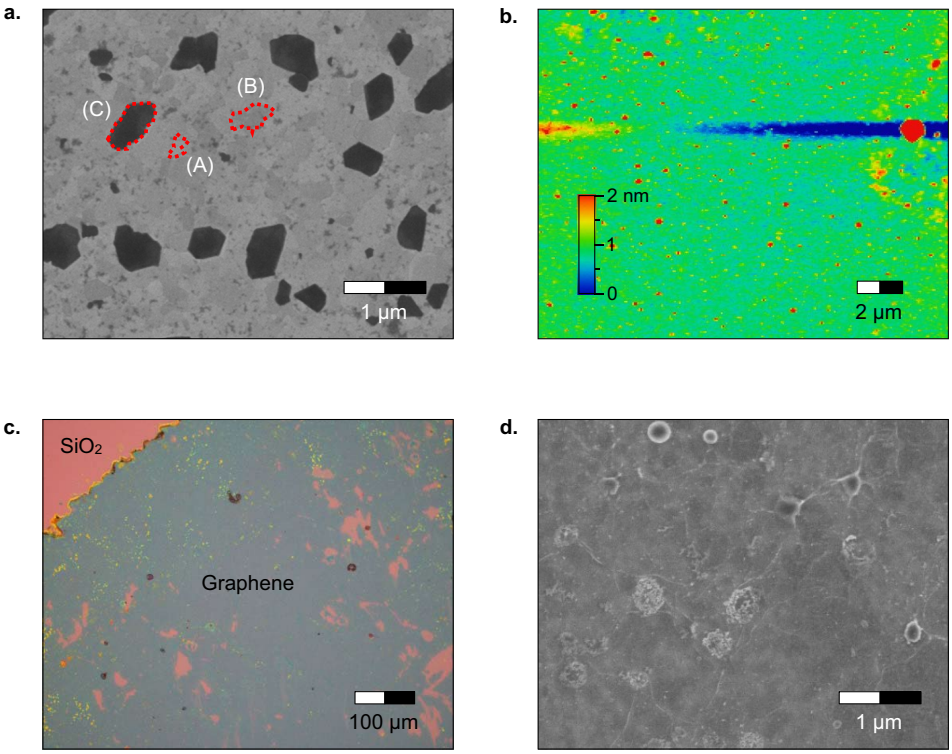

Fig. 3 Surface morphology of graphene grown on Pt thin-films. **a** SEM and **b** AFM images of a graphene film on 100 nm Pt after CVD growth. **c** Optical microscopy and **d** SEM images of graphene grown on 50 nm Pt and transferred onto an oxidized Si wafer. Note, despite using graphene grown on Pt layers with different thickness (i.e. 100 nm for **a**, **b** and 50 nm for **c**, **d**), the catalyst thickness did not affect the quality of graphene according to Raman spectroscopy (Fig. 2)

thin-films were transferred onto oxidised Si wafers. The optical contrast of graphene on SiO_2 (i.e. without catalyst underneath) depends on the SiO_2 thickness [53] and is much higher compared to graphene on a metal layer such as Pt. This allows to analyse the transferred graphene layer on SiO_2 by optical microscopy as shown in Fig. 3c. The image reveals that a large area multilayer graphene film has been grown on the Pt thin-film. The small cracks and holes are due to damages during bubbling transfer. A SEM image of a transferred graphene layer is shown in Fig. 3d. Apart from surface contamination and the cracks caused by the bubbling transfer, the film appears to be homogenous on the microscale.

3.2 Graphene growth on Pt–Cu thin-film heterostructures

Proton selective transport through graphene [54] could be used to control the formation of counter charges [55–61] at the inert Pt electrode, which are required for resistive switching. By passivation of the electrochemical active Cu electrode, unintentional ion injection of cations into the switching layer could be suppressed. In this context, graphene has already been used to selectively tune the ionic transport from the electrochemical active electrode [26]. Thus, both passivation of the Cu and Pt electrode is technologically of interest. However, a direct growth of graphene on copper thin-films using the aforementioned adhesion layer is technologically difficult due to the thermally enhanced diffusion of copper into oxides even at relatively low temperatures like 400 °C [62, 63]. Thus, the high process temperature during CVD growth will cause significant Cu diffusion and electrode degradation. To overcome this problem, we evaporated Cu on Pt thin-films and make use of the thermal stability of the Pt thin-films during graphene growth.

Figure 4a depicts Raman spectra of graphene grown at 800 °C on 60 nm Cu thin-films deposited on 30 nm and 100 nm Pt thin-films (Pt–Cu heterostructures), respectively. The Raman spectra are very similar to the Raman spectra of graphene layers grown directly on Pt (Fig. 2). The D/G-ratio is 0.75 for the 30 + 60 nm Pt–Cu catalyst and 0.81 for the 30 + 100 nm Pt–Cu catalyst, respectively. Higher temperatures than 800 °C were not used for graphene growth on Pt–Cu heterostructures. But we assume that the D/G-ratio may be reduced at higher temperatures similar to the results for pure Pt thin-films. However, special attention needs to be paid to potential dewetting in this case.

We also analysed the chemical composition of the Pt–Cu heterostructures after growth by EDX (Fig. 4b). We do not observe any significant change of the spectrum of Pt or Pt–Cu thin-films after growth compared to unprocessed reference layers. However, EDX is not surface sensitive, and we do not get any information regarding a Cu gradient across the Pt–Cu heterostructures. But we expect

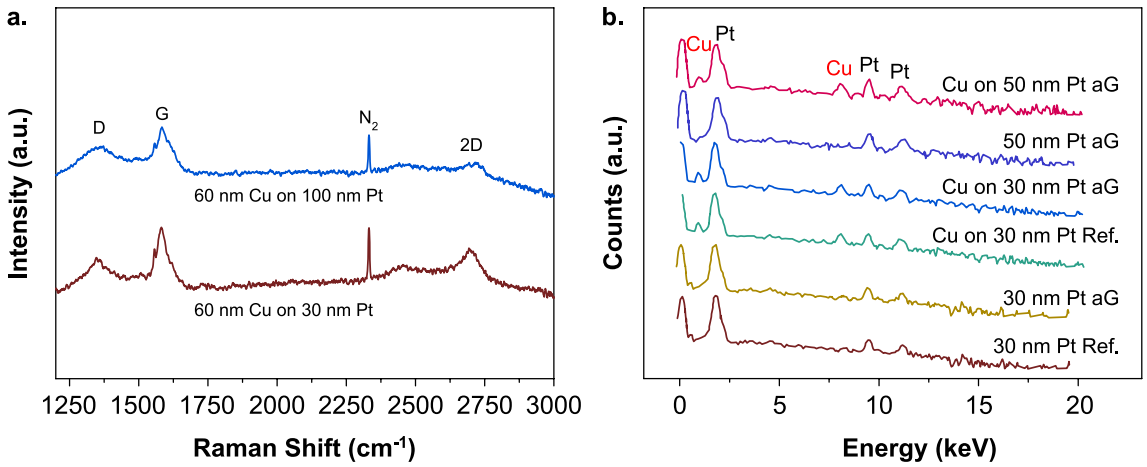

Fig. 4 Characterisation of Pt–Cu heterostructures for CVD growth of graphene. **a** Raman spectra of graphene grown at 800 °C on 30 + 60 nm Pt–Cu (red) and 100 + 60 nm Pt–Cu (blue) thin-films. **b** EDX spectra of the Pt–Cu-graphene heterostructure after CVD growth (aG) in comparison of unprocessed reference layers

that at relatively high temperatures like 800 °C Cu will most likely form an alloy at the interface with the Pt thin-film [64–66]. We expect that this is not critical for memristive switching as long as a sufficient amount of Cu is available at the interface to the switching material for anodic oxidation. Since nanoscale Cu filaments are formed during device operation, only a small amount of Cu atoms (typically in the order of 10^6 atoms) is required for memristive switching. In fact, the use of alloys for the anode has already demonstrated improved switching performance [67].

3.3 Impact of deposition of memristive oxides on graphene

In memristive devices the integrated graphene passivation (either on Pt or Pt–Cu) will be in contact to the switching material, which is typically an oxide or higher chalcogenide. In this case, the deposition process of the memristive material can degrade or even damage the graphene passivation.

Atomic layer deposition is a widely used method to grow oxides on graphene without degradation of the 2D material [68]. Since graphene is fairly hydrophobic, ALD growth is facilitated at defects and grain boundaries. This only allows for growth of relatively thick oxides thin-films (some tens of nanometre). These films are much thicker (typically ≫ 50 nm) compared to the typical thickness of memristive switching layers (usually between 10 to 50 nm). However, much thinner and yet homogenous layers (i.e. ≪ 10 nm) can be grown by special ozone treatments [46]. Physical vapor deposition (PVD) based on radio-frequency sputtering is a common method for fabrication of memristively switching oxides, e.g. Refs. [69, 70]. However, integration of graphene in metal/oxide heterostructures is difficult when the oxide is prepared on-top of the graphene layer by sputter deposition, because the kinetic energy of the sputter-atoms can damage the graphene layer. To overcome this challenge, Qiu et al. made a comprehensive study on sputter deposition of thin-films on graphene and found that a high Ar pressure allows for significant reduction of the level of damage to graphene [71]. Besides sputter deposition, e-beam evaporation (which is also a PVD process) [72–75] as well as PECVD [76, 77] are established methods for fabrication of memristively switching oxides as well. Here we analyse the quality of transferred graphene after oxide deposition (e-beam deposition, PECVD and ALD) by Raman spectroscopy. As model materials we used SiO_2 and Ta_2O_5 since these materials are well-studied and fabrication friendly [78]. For e-beam deposition of SiO_2 and Ta_2O_5 we used the same method and process parameters that have been used for fabrication of SiO_2- and Ta_2O_5-based ECM devices [73, 75, 79]. Besides e-beam evaporation, PECVD grown SiO_2 has been also used for fabrication of memristive devices by other groups in the past [76, 77]. For comparison, Al_2O_3 has been deposited using an established ALD process [46] as reference. Previously, A. Sokolov et al. reported on memristively switching ALD-grown Al_2O_3 thin films [80]. Hence, the selected oxides (SiO_2, Ta_2O_5 and Al_2O_3) and deposition methods are relevant for fabrication of memristive devices.

Figure 5 depicts Raman spectroscopy results for transferred graphene layers grown on Cu foils with electron-beam evaporated SiO_2 and Ta_2O_5 thin-films (thickness between 30 and 50 nm, respectively, Fig. 5a), and ALD grown Al_2O_3 (thickness 10 nm) and PECVD grown SiO_2 (20 nm) for comparison. Note, the oxides were deposited after the graphene layers have been transferred onto a Si/

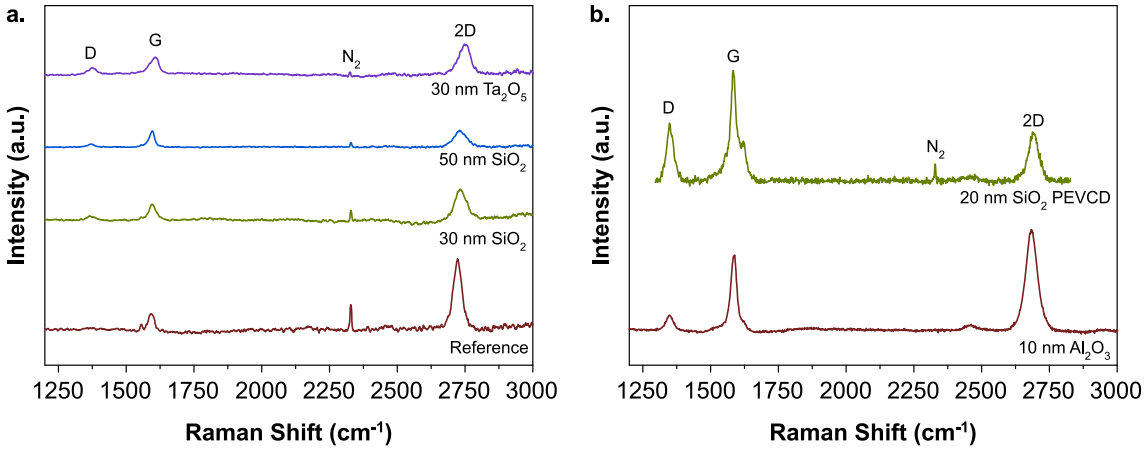

Fig. 5 Raman spectroscopy of graphene after **a** e-beam deposition of SiO_2 and Ta_2O_5 thin-films, and **b** 10 nm Al_2O_3 deposited by ALD and 20 nm SiO_2 deposited by PECVD, respectively. The Raman spectrum of transferred graphene grown on a Cu foil without further processing (Reference) is shown for comparison in (**a**)

SiO_2 substrate (without TiO_2 and intermediate Pt or Pt–Cu layer), which allows us to selectively analyse the impact of the oxide deposition on the graphene layer. Beside the appearance of the D peak, the 2D peak also reveals information about the morphology and defects of the graphene layer in a non-trivial way. We used a bubbling transfer process, which allows for transfer of high-quality graphene [38]. Thus, we can ensure that potential defects of the graphene/oxide heterostructures in Fig. 5 are only caused by the oxide deposition. The Raman spectrum of graphene after growth and transfer without any subsequent oxide deposition (reference sample) is shown in Fig. 5a. Here, the D peak height is insignificant compared to the G peak (i.e. minimal defects are expected from the D/G-ratio) and the full width at half maximum (FWHM) of the 2D peak is about 32–35 cm^{-1} (24 cm^{-1} are expected for nearly defect free suspended graphene) [47]. When SiO_2 is evaporated on top of graphene, the D/G-ratio varies between 0.17 and 0.25, which is relatively small. This indicates long defect distances (> 20 nm) [50]. While the G peak remains at 1582 cm^{-1} for all SiO_2 samples, the 2D peak is shifted by 10 cm^{-1} and its FWHM is about 45–54 cm^{-1}. In case of Ta_2O_5 the D/G-ratio is 0.33, which is larger compared to the SiO_2 samples. Furthermore, both the G and 2D peak are shifted by about 18 and 34 cm^{-1}, respectively. The FWHM of the 2D is again about 57 cm^{-1}. A similar trend is observed for ozone-assisted ALD grown Al_2O_3 on graphene (Fig. 5b). Here, the D/G-ratio is 0.22 and for PECVD SiO_2 on graphene 0.53. Thus, we conclude that the oxide deposition by e-beam evaporation, ALD and PECVD induced a small yet detectable amount of defects, regardless if SiO_2, Ta_2O_5 or Al_2O_3 is deposited. In case of PECVD plasma seems to induce more defects than e-beam evaporation and ALD. Nevertheless, the graphene layer is still intact and can be used as passivation.

3.4 Discussion on the role of defects and crystallinity on the passivation layer quality

The most important advantage of the grown passivation layers is that they are ultra- or even atomically thin. This results in a significantly lower voltage drop across the passivation layer compared to a voltage drop across conventional passivation layers based on thin-films. A lower voltage drop is beneficial for low-power operation of the memristive device. We expect that the passivation layer with highest quality would be a defect-free mono-crystalline atomically thin 2D material. Such a material may allow to change the ionic penetration of the passivation layer at any arbitrary location by deliberately forming defects using e.g. nano-focussed electron-beams [81–83].

Growth of large-area mono-crystalline graphene has been demonstrated on single-crystal hydrogen-terminated Ge substrates [84]. But growth of almost defect-free graphene layers on polycrystalline catalyst layers remains challenging. Thus, besides the thickness, the crystallinity and defect concentration of the passivation layer may be also important. Among the most important defects in graphene are grain boundaries [85]. Thus, the crystallinity (i.e. grain size) and defect concentration may be correlated to some degree. In this context, Cançado et al. reported that the D/G-ratio increases by decrease of the grain size [86]. This can be explained by grain boundaries, which are two-dimensional defects [87], becoming more relevant as the grain size decreases. In this study, the grain size is relatively small (in micrometre-scale or even smaller). We assume

that the small grain size is due to the small grain size of the Pt catalyst. As mentioned above, the D/G-ratio can be slightly reduced by using higher CVD process temperatures. In this study the D/G-ratio of graphene layers grown at 800 °C is approximately twice as high as the D/G-ratio of graphene layers grown at 920 °C. However, at such high temperatures we observed first indication of dewetting of the catalyst on some samples. Another way to facilitate the growth of larger graphene grains may be to design catalyst with larger grains. However, the grain size of the catalyst is here limited by the thickness of the Pt thin-film [88]. Based on Fig. 5 it is also important to consider defects induced by deposition of thin-films on the passivation layer.

In case crystallinity plays a minor role in terms of the quality of the passivation layer, a completely different approach would be to grow amorphous carbon monolayers [89–91]. The advantage of the growth of amorphous carbon monolayers is the lower substrate temperature (200–500 °C), which further reduces the risk of dewetting. But the ionic permeability of amorphous carbon monolayers has not been investigated so far. Thus, the applicability of amorphous carbon monolayers for passivation of ECM-electrodes is yet unclear.

4 Conclusions

In this study we demonstrated the CVD growth of graphene on Pt thin-films and Pt–Cu heterostructures for process temperatures of 800 °C without dewetting of the metal catalyst. The graphene layers have small grain sizes reflecting the grain sizes of the catalysts. They are fairly defective but fully covering the catalyst surface. The defect concentration can be reduced by higher CVD process temperatures (here 920 °C). However, in this case we found indications of dewetting of the Pt thin-films. Nevertheless, the demonstrated process allows for fabrication friendly and large-scale passivation of Pt–Cu and Pt thin-films. In follow-up studies based on the optimized adhesion layer, integration of alternative 2D-materials in RRAMs, in particular insulating two-dimensional hexagonal boron-nitride, could be evaluated. Moreover, besides ALD we found that graphene layers are withstanding e-beam and PECVD deposition of selected oxides like SiO_2, Ta_2O_5 and Al_2O_3 thin-films, which are relevant for memristively switching devices. The demonstrated new integration path is scalable and opens up systematic future studies on improved switching characteristics. The method here also extends to other 2D material, such as 2D h-BN.

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Data availability The data that support the findings of this study are available on request from the corresponding author.

Declarations

Conflict of interest The author has no conflict to disclose.

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